Phase Tracking Electronically Variable Attenuators with Receiver Protection

by

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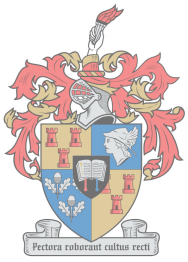

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Abstract

This dissertation presents the development of a set of optimal phase tracking electronically variable attenuators. Secondly, a compact high power PIN diode limiter is developed and its minimum attainable resistance is extracted through high power measurements.

Close range reflections cause the receiver of a multi-channel digital beamforming radar to saturate. Controlled attenuation over time, implemented with electronically variable attenuators, is used to prevent receiver saturation (sensitivity time control). An electronically variable attenuator is placed in front of the first low noise amplifier in each channel; its insertion loss directly adds to the receiver's noise figure.

A multi-channel digital beamforming radar receiver requires good phase tracking between its receiver channels to minimise direction of arrival estimation errors. The set of electronically variable attenuators used for sensitivity time control need to track in phase over the control range. In this dissertation, sensitivity analysis is used to identify a set of optimal phase tracking electronically variable attenuators. A root sum square error measure is derived from the multiple output sensitivities of an electronic network. The error measure gives the expected RMS phase error within a set of networks. Applying the error measure to several electronically variable attenuators over the control range, the cascaded parallel quarter-wave attenuator is identified as having optimal phase tracking within a set of attenuators over control range. The cascade parallel quarter-wave attenuator is developed further and optimised through the application of sensitivity analysis. The final attenuator has excellent attenuation flatness, attenuation range, phase tracking and a simple biasing scheme.

A multi-channel digital beamforming radar receiver also has to be protected against large signals. These large potentially damaging signals are either due to the radar's own transmitted signal, or from other radars transmitting large amounts of power in the same frequency band. A receiver protector (e.g. a limiter) typically supplies this function.

In a multi-channel digital beamforming radar, a compact circuit based high power limiter has many advantages in terms of space and cost when it is compared to a waveguide limiter. The compact high power limiter developed in

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this dissertation consists of PIN diodes implemented on a multi-layer printed circuit board. The circuit is referred to as an active PIN-Schottky limiter. The maximum power handling capability of the active PIN-Schottky limiter is determined by the PIN diode at the limiter's input. The minimum attainable resistance is not given by the manufacturers, so that the diode's minimum attainable resistance can not be found from the datasheet information. It is difficult to estimate how much power is dissipated in the diode when a large signal is incident. Through a temperature controlled measurement, the PIN diode's voltage decrease as a function of junction temperature increase is measured. By fitting the PIN diode's measured and simulated junction temperature increase, it is possible to extract the resistance of the diode when large forward bias is applied. Once the resistance is known, the power dissipated in the PIN diode can be calculated for different operating conditions.

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Uittreksel

In hierdie proefskrif word 'n stel van optimale fasesporende elektronies verstelbare verswakkers ontwikkel. Tweedens word 'n kompakte hoëdrywing PIN diode beperker ontwikkel. Die beperker se maksimum drywing hanteringsvermoë word bepaal deur die PIN diode se minimum haalbare weerstand te onttrek met hoëdrywing metings.

Naby teikens veroorsaak onvanger versadiging in 'n multi-kanaal digitale bundelvormende radar. Beheerde verswakking oor tyd, geïmplementeer deur elektronies verstelbare verswakkers, voorkom ontvanger versadiging (sensitiwiteits tyd beheer). 'n Elektronies verstelbare verswakker word voor die eerste lae ruis versterker in elke ontvanger kanaal geplaas; die inset verlies word direk by die ontvanger se ruissyfer getel.

Multi-kanaal digitale bundelvormende radar ontvangers benodig goeie fasesporing tussen die verskillende kanale om foute in die teiken rigting skatting te voorkom. As 'n stel van elektronies verstelbare verswakkers gebruik word om sensitiwiteits tyd beheer toe te pas, moet die stel van verswakkers ook spoor in fase oor die verswakking bereik. In hierdie proefskrif word sensitiwiteitsanalise gebruik om 'n stel van fasesporende elektronies verstelbare verswakkers te identifiseer. 'n Wortel kwadraat som foutmaatstaf word afgelei van 'n elektroniese netwerk se veelvuldige uittree sensitiwiteite. Die foutmaatstaf gee die verwagte wortel gemiddelde kwadraat (WGK) fasefout binne 'n stel van elektoniese netwerke. Die fasefout van verskeie aangepaste elektronies verstelbare verswakkers word bereken en die kaskade parallel kwartgolf-lengte verswakker word geïdentifiseer as die topologie met optimale fasesporing binne 'n stel van verswakkers oor die verswakkingsbereik. Deur die toepassing van sensitiwiteitsanalise word die kaskade parallel kwartgolf-lengte verswakker se werksverrigting verder ontwikkel en geoptimiseer. Die kaskade kwartgolf-lengte verswakker het uitstekende verswakking platheid, verswakking bereik, fasesporing en 'n eenvoudige voorspanningskema.

'n Multi-kanaal digitale bundelvormende radar benodig ook beskerming teen skadelike seine afkomstig van die radar se eie sender, sowel as drywing wat uitgesaai word deur ander radars in dieselfde frekwensieband. 'n Ontvanger beskermer (bv. 'n beperker) word tipies vir hierdie toepassing gebruik.

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Dit is baie meer voordelig om 'n kompakte beperker te gebruik in plaas van 'n golfleier beperker in 'n multi-kanaal digitale bundelvormende radar in terme van prys en spasie in die ontvanger. Die kompakte hoëdrywing beperker wat hier bespreek word bestaan uit PIN diodes wat geïmplementeer is op 'n multi-laag gedrukte stroombaanbord. Die PIN diode beperker beskerm die ontvanger teen beide sy eie sender drywing (aktief) en ander radars se seine (passief). Die maksimum drywing hanteringsvermoë van die beperker word bepaal deur die minimum haalbare weerstand van die eerste PIN diode. Verskaffers gee nie die PIN diode se minimum weerstand nie, sodat die minimum haalbare diode weerstand nie gevind kan word uit datablad inligting nie. Dit maak dit moeilik om die maksimum intreedrywing van 'n spesifieke beperker opstelling te bepaal. 'n Temperatuur beheerde toetsopstelling word gebruik om die afname in PIN diode spanning te meet vir toenemende vlaktemperatuur. Die gemete vlaktemperatuur word vergelyk met 'n termiese model van die PIN diode. Die PIN diode se minimum haalbare weerstand word onttrek deur die gemete en gesimuleerde vlaktemperatuur te pas. As die PIN diode se minimum haalbare weerstand bekend is, kan die drywing wat die diode verkwis bereken word vir verskillende werkstoestande.

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Nomenclature

Abbreviations

CPQA	Cascade parallel quarter-wave attenuator
CSQA	Cascade series quarter-wave attenuator
CW	Continuous wave
DBF	Digital beamforming
EVA	Electronically variable attenuator
I	In phase
LNA	Low noise amplifier
PCB	Printed circuit board
Q	Quadrature
RF	Radio frequency
RMS	Root mean square
RSS	Root sum square
SMA	Sub miniature type A
STC	Sensitivity time control
VNA	Vector network analyser

Constants

c =	$3\text{x}10^{8}\text{m/s}$
ϵ_0 =	$8.854\text{x}10^{-12}\text{F/m}$
μ_0 =	$4\pi\text{x}10^{-7}\text{H/m}$
ρ_{CU} =	$3960\mu\text{J/}^{\text{o}}\text{C}$
σ_{CU} =	385W/Km
c_{θ_CU} =	3885J/Kkg

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Chapter 1

Introduction

This dissertation documents the development of a receiver protector that provides large signal protection and sensitivity time control to a multi-channel receiver of a digital beamforming (DBF) radar.

The contributions presented in the dissertation are divided into two parts. Firstly, a purpose made root sum square (RSS) phase error measure is derived from output sensitivity results. The RSS phase error measure gives the phase error that exists within a set of networks due to component tolerances. Using the RSS phase error measure, an optimal phase tracking set of electronically variable attenuators is developed for a multi-channel receiver.

The second set of contributions is focused around the design of a compact high power limiter. The limiter's power handling capabilities are characterised through its PIN diode temperature response. Sensitivity analysis is used to optimise the limiter's reflection coefficient. An improvement to the limiter's passive reverse recovery time is proposed.

1.1 Problem description

1.1.1 Multichannel DBF radar

A multi-channel DBF radar determines the direction of arrival (DoA) of reflected signals by calculating the phase difference between signals received on multiple receiver channels. Fig. 1.1 shows an n channel DBF radar transceiver. A circulator isolates the receiver from the transmitter.

Typically, a PIN diode limiter is used as a receiver protector in high power applications. Limiters use PIN diodes to block large incoming signals by presenting an impedance mismatch to the incident signal.

The high frequency small signal model of a PIN diode is shown in Fig. 1.2. A further description of the PIN diode's small signal model is given in Chapter 2.

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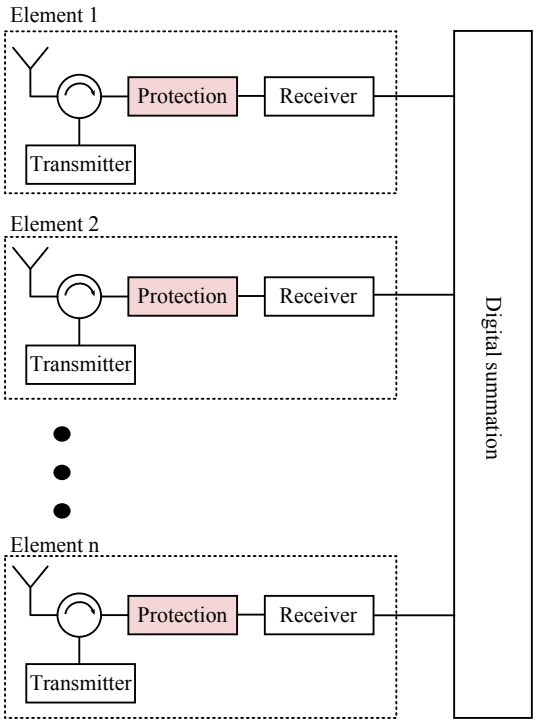

Figure 1.1: Block diagram of DBF radar front end.

In a large signal environment, a multi-channel receiver needs receiver protectors to protect sensitive components in the receiver chain, as indicated in Fig. 1.1. As an example, if the transmitter generates a 1 kW peak output signal to the antenna, and the antenna has a reflection coefficient of -10 dB, the antenna reflects 100 W towards the receiver.

Designing a limiter presents several challenges. A limiter's reaction time to large incoming signals determines whether it effectively protects the receiver. If the spike leakage exceeds the maximum power of sensitive components further down the receiver chain, the limiter has failed in its function. The time the limiter takes to recover after the limiting cycle has ended determines the

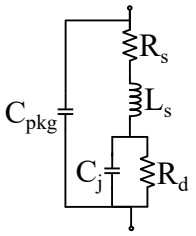

Figure 1.2: High frequency small signal model of a PIN diode. R_d is the current controlled resistance, R_s is the PIN diode's N layer and bond wire resistance, C_j is the junction capacitance, L_s is the bond wire inductance and C_{pkg} is the package capacitance [1].

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minimum time before the radar can detect another target. Clearly, a fast recovery time is important.

A limiter's performance is measured by:

1. How fast it reacts to a large incident signal (starts protecting).
2. How much it isolates the receiver from the large signal (amount of protection in dB).
3. How fast it can recover to normal operating conditions once the large signal has passed.

A limiter's maximum power handling capability is dictated by the maximum power that can be dissipated in its PIN diode. In turn, the PIN diode's maximum power handling ability depends on its minimum resistance ($R_s + R_d(@Imax)$) in Fig. 1.2).

Waveguide receiver protectors can handle more power than a PIN diode limiter. However, in a multi-channel receiver where the use of additional space is not an option, a large structured limiter could cause an unacceptable increase in cost. A compact high power limiter is needed that can protect a receiver from large signals that are reflected from the antenna during the transmit cycle, as well as unexpected damaging signals received by the radar.

In compact limiter design, a challenge that needs to be overcome is the maximum power that can be dissipated in a plastic packaged surface mount PIN diode. Often, there is not enough initial information to correctly characterise the high power performance of the limiter. The power handling requirements of a compact microstrip limiter are discussed further in Section 1.1.2.

Supplementary to the blocking function of a limiter, controlled attenuation over time is also provided and is referred to as sensitivity time control (STC).

Controlled attenuation over time is applied before the first low noise amplifier (LNA). Insertion loss before the LNA adds directly to the receiver's noise figure. As a result, the attenuation circuit should have minimal insertion loss when STC is not applied. Digital attenuators typically have insertion loss larger than 2 dB.

Electronically variable attenuators (EVA) use PIN diodes as current controlled resistors at high frequencies. Unlike the limiter, an EVA biases a PIN diode over its full control range. PIN diodes present a varying complex impedance over its control range. The PIN diode's changing complex impedance alters the EVA's transmission phase response from the ideal response. As the EVA's transmission phase changes over control range, the phase tracking error between channels due to component tolerances vary.

Good phase tracking between channels is often a requirement for multi-channel receivers. Component and transmission line dimensional tolerances cause variations in phase tracking between channels in a multi-channel receiver.

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To reduce phase tracking errors, an EVA has to be matched at its input and output ports. Signals re-reflected from external circuitry contribute to phase errors. Small variations in a PIN diode's complex impedance for a given PIN diode resistance can cause phase tracking errors within a set of networks. Additionally, dimensional tolerances of transmission lines also contribute phase tracking errors. An ideal EVA for a multi-channel receiver will have minimised phase tracking errors over the control range within a set of attenuators. Section 1.1.3 illustrates the effect of phase tracking errors in the DoA estimation for a two channel receiver.

Clearly, the protection and attenuation control of a multi-channel receiver consists of two parts: a limiter that provides large signal protection, and an electronically variable attenuator that also gives protection through controlled attenuation over time. In this dissertation:

1. A compact high power limiter has to be developed to protect a receiver. Most importantly, the PIN diode limiter's maximum power handling capability has to be characterised.

2. An EVA with minimal phase error sensitivity has to be developed. A method to rank the phase tracking ability of any given electrical network is needed. This method can be used to compare and ultimately identify an optimal set of phase tracking EVAs over their full control range.

1.1.2 Power handling of a microstrip limiter

A limiter protects a receiver by either reflecting or absorbing large damaging signals. Forcing a PIN diode to dissipate a substantial fraction of a large incoming signal limits the maximum power handling ability of the limiter. Forward biased parallel connected PIN diodes reflect the bulk of the unwanted power. As a result, the power handling requirement of the reflecting element is only a fraction of the incident power.

Fig. 1.3 shows a typical two-stage detector PIN diode limiter. A Schottky diode is used to lower the PIN diode's limiting threshold [2]. The directional coupler couples a portion of the input power that forward biases the the Schottky diode D_2 and in turn biases PIN diode D_1 through L_{RF}. By using a directional coupler the Schottky diode's breakdown voltage requirement is lower.

The configuration with a directional coupler in Fig. 1.3 is more typical of higher power limiters. For medium power limiters, the current rectified by the Schottky diode through the coupler is too small to effectively bias its PIN diode. An amplifier can be used to increase the current rectified by the Schottky diode. This topology would require a power source to provide protection.

The total power dissipated in a PIN diode is a function of the total minimum resistance of the PIN diode. As power is dissipated in the PIN diode,

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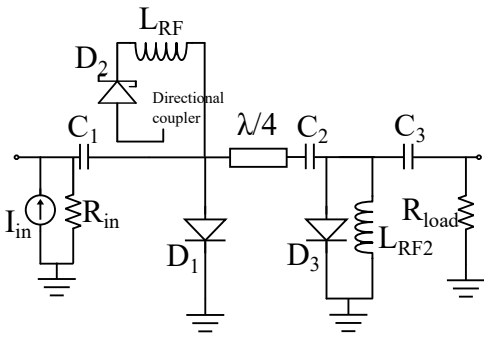

Figure 1.3: Typical two-stage detector PIN diode limiter, similar to the limiter in [2]. D_1 is the 'coarse' limiter PIN diode, D_2 is a Schottky diode and D_3 is the 'clean up' PIN diode. L_{RF} and L_{RF2} are RF chokes used to form a DC current path [2].

its junction temperature increases. A PIN diode limiter reaches its maximum input power limit when its junction temperature has increased to a critical value.

A PIN diode's junction temperature can be managed through good heat transfer. The maximum input power given on a PIN diode's datasheet is typically when heat transfer from the PIN diode's junction to ambient is optimal.

If the minimum resistance of a PIN diode is not known, it is impossible to predict how much power can be applied to the limiter without catastrophic PIN diode junction heating.

The PIN diode's minimum resistance, power dissipated and consequently junction temperature increase, are often design unknowns.

1.1.3 Phase tracking error and DoA estimation

Fig. 1.4 shows a linear array of two receivers with equally spaced isotropic antennas illuminated by a sinusoidally varying wave reflected from a target [3]. Assume the antennas are noiseless. A plane wave is incident from a direction θ to the axis of the array. The wave travelling to the antenna array will reach each antenna element at a different time (phase position). If the antenna element at position 0 in Fig. 1.4 is chosen as the origin, the direction of arrival of the wave can be calculated by the phase difference measured between the waves received at the different channels:

$$\Delta R_n = nD\cos\theta \tag{1.1.1}$$

where $n = 0, 1$ for a two element receiver [3].

The instantaneous electric field of the plane wave with frequency f and wavelength $\lambda = \frac{c}{f}$ that is incident on an antenna is given by the electrical field vector $\tilde{e}(t)$. The electrical field vector is a function of time and distance from

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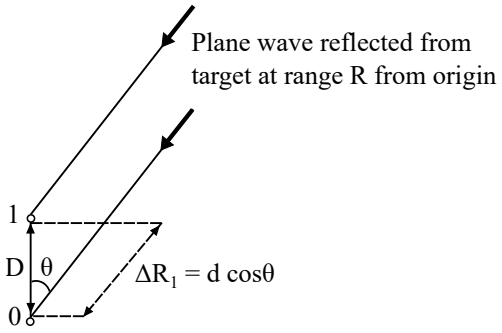

Figure 1.4: Two element receiver with equally spaced isotropic antennas. A plane wave is incident from a direction specified by the angle θ.

the source:

$$\tilde{e}(t) = E_0 \exp\left[j\left(-\frac{2\pi r}{\lambda} + 2\pi f t + \psi_0\right)\right] \tag{1.1.2}$$

where E_0 is the peak amplitude of the field, r is the distance travelled in the direction of propagation from some reference point and t is the time. ψ_0 is a phase angle dependent on the instant used as a time reference and the reference position.

Considering the n antenna elements in Fig. 1.4, the electric field can be written as a time varying phasor with unity amplitude $s[n, \theta]$. The signal phasor received at element n with reference to the origin is given by:

$$s[n, \theta] = \exp\left(j\frac{2\pi D n \cos\theta}{\lambda} + j\psi_0\right) = \exp\left(j\{\psi[n]\}\right) \tag{1.1.3}$$

The phase $\psi[n]$ of the phasors received at the two elements in Fig. 1.4 are $\psi[0] = \psi_0$ and $\psi[1] = \frac{2\pi d \cos\theta}{\lambda} + \psi_0$.

Consider a two-channel receiver with components in each channel that add randomly varying noise to the incoming signal. Without loss of generality, ψ_0 can be set to zero, and amplitude noise can be ignored. The phase noise is represented by an RMS quantity $\tilde{\psi}_{n1}$ and $\tilde{\psi}_{n2}$, and is added to Eq. 1.1.3's phase when $n = 0, 1$ respectively. The phase of the two elements in Fig. 1.4 now become:

$$\begin{aligned} \psi[0] &= \tilde{\psi}_{n1} \\ \psi[1] &= \frac{2\pi D \cos\theta}{\lambda} + \tilde{\psi}_{n2} \end{aligned} \tag{1.1.4}$$

To determine the DoA, the phase difference $\Delta\psi$ between the two elements in Fig. 1.4 is calculated for no noise:

$$\Delta\psi = \psi[1] - \psi[0] = \frac{2\pi D \cos\theta}{\lambda} \tag{1.1.5}$$

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By taking the derivative of $\Delta\psi$ with respect to the DoA angle θ:

$$\begin{aligned} \frac{d\Delta\psi}{d\theta} &= \frac{-2\pi D \sin\theta}{\lambda} \\ d\theta &= \frac{-\lambda}{2\pi D \sin\theta} d\Delta\psi \end{aligned} \tag{1.1.6}$$

If $\Delta\psi$ has an RMS noise $\tilde{\psi} = \sqrt{\tilde{\psi}_{n1}^2 + \tilde{\psi}_{n2}^2}$, the RMS DoA deviation is given by:

$$\tilde{\theta} = \frac{\lambda}{2\pi D \sin\theta} \tilde{\psi} \tag{1.1.7}$$

This equation also holds for small phase tracking errors.

1.1.4 Developing a set of phase tracking networks

To develop an optimal phase tracking set of networks, a method for grading networks in terms of their phase tracking has to be developed. The major contribution to phase tracking errors are:

1. Variations in the complex impedance of different PIN diodes.
2. Dimensional tolerance errors in manufactured transmission lines.
3. Variations in element values of discrete components.

Sensitivity analysis gives the relative change in output due to small variations in component value [4]. By using sensitivity analysis, the output error can be determined for variations in element values in a network. The existing sensitivity equations have to be extended to include errors due to transmission line tolerances. Additionally, the multiple output sensitivities have to be interpreted to give a single comparable phase tracking error for given tolerance errors in a network.

A matched EVA typically consists of transmission lines, discrete elements and PIN diodes. Microstrip transmission lines contain uncertainties regarding the substrate's relative dielectric constant that results in line impedance and propagation constant variations. Substrate height tolerance cause variations in characteristic impedance, which could cause phase tracking errors within a set of networks.

Output sensitivity results are developed further to determine a single error measure with which to rank different networks in terms of phase errors. By using a single error measure, an optimal set of phase tracking EVAs is identified.

This dissertation documents the development of a set of optimal phase tracking EVAs that will result in a minimum randomly varying phase error in a multi-channel system's DoA estimation. Additionally, a high power compact limiter designed, and a high power method is used to determine its power handling ability.

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1.2 Project contributions

1.2.1 Contribution 1

Extend existing sensitivity analysis of lumped networks to create a generalised framework that accommodates both lumped and distributed elements. Use the sensitivity results to improve circuit performance.

Sensitivity analysis is not a new concept. In this dissertation a novel approach using sensitivity analysis is derived to create a tool with which networks consisting of lumped and distributed elements can be analysed. Additionally, sensitivity analysis is performed without constructing an adjoint circuit.

The proposed sensitivity analysis takes into account variations in distributed transmission lines with respect to propagation delay and characteristic impedance. These variations occur due to relative dielectric constant and substrate height tolerances. This method of analysis provides a unique insight into the effects of the components in the circuit on both the EVA's input and output responses.

By applying sensitivity analysis to the limiter's small signal model, the sensitivity results contribute valuable insights that aid in the optimal small signal design of the circuit.

1.2.2 Contribution 2

Define an effective sensitivity error measure from the sensitivity results, suitable to rank the phase tracking performance of multiple electronic networks.

Sensitivity analysis reflects a change in an output quantity for each circuit variable (tolerance, temperature dependence). To rank different types of networks in terms of phase tracking, a single error measure is needed. Taking the square root of the sum of the squared output variations, a single error measure is determined. With due regard to correlated variations, this error measure shows the expected RMS phase error within a set of networks due to component tolerances.

1.2.3 Contribution 3

Use the defined error measure to critically examine and compare the phase tracking performance of several PIN diode EVAs to identify an optimal phase tracking topology.

There are many EVA topologies. To identify a topology that has optimal phase tracking performance, the error measure that was derived from sensitivity results is used to rank different topologies. This error measure shows the expected RMS phase error in output due to component tolerances, which also indicates the phase variation that will occur within a set of matched EVAs. By

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analysing a selection of matched EVAs, the topology with the smallest phase error measure will have optimal phase tracking performance.

The novelty of the identified phase tracking EVAs lies in a combination of excellent transmission and reflection characteristics and optimal phase tracking performance. The need for a set of EVAs with good phase tracking has resulted in the design of a more compact topology that improves on currently available attenuators for the given specifications. The EVA topology proposed here contains a particular combination of simplified biasing network, attenuation range, attenuation flatness, and optimal phase tracking.

Developing an EVA with optimal phase tracking within a set of EVAs that also has low insertion loss is important for multi-channel DBF radar receivers. Since EVAs are used before the first LNAs, the insertion loss of the EVA adds directly to the receiver's noise figure. Using commercially available digital attenuators with good phase tracking is not a viable solution since they typically have large insertion loss. The optimal phase tracking EVA developed in this dissertation also has low insertion loss.

1.2.4 Contribution 4

Develop an approach using high power measurements to characterise a high power limiter.

PIN limiter diodes are often specified with a resistance at a single forward current. This value consists of both the I region resistance and the resistance contributed by the N and P layers. The PIN diode's minimum attainable resistance is limited by the N and P layer resistance.

It is difficult to measure the true minimum resistance of a PIN diode using small signal measurements. The value is typically masked by the diode's series inductance in a grounded surface mounted configuration.

Without knowledge of a PIN diode's minimum resistance, it is impossible to calculate the maximum power that can be dissipated in a PIN diode. The approach discussed in this dissertation first measures the PIN diode's forward voltage versus junction temperature increase under zero RF conditions. Once the temperature rise for a given high power input is known, a thermal model of the PIN diode junction's heat removal can be fit to measured data. By fitting the measurements to the simulation, it is possible to estimate the minimum attainable resistance of the PIN diode.

1.2.5 Contribution 5

Improving the passive PIN-Schottky diode limiter's reverse recovery time.

It is well documented that the reverse recovery time of a PIN-Schottky limiter is extremely slow. Through the addition of a single resistor it is possible

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to drastically improve the reverse recovery of the limiter's passive operation without affecting other operation.

1.3 Project layout

Chapter 2 contains a literature review of PIN diodes, limiters and matched EVAs.

Sensitivity analysis as a method to rank electrical networks in terms of phase tracking is discussed in Chapter 3.

Chapter 4 compares different variable attenuator topologies. By using the sensitivity analysis method developed in Chapter 3, an optimal phase tracking set of EVAs is identified.

Chapter 5 documents the process of designing a high power limiter. The high power measurement method used to extract a PIN diode's minimum attainable resistance is discussed.

The final conclusions are given in Chapter 6.

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Chapter 2

Literature Review

2.1 Introduction

In this dissertation, two modules for use in a multi-channel receiver are developed: a set of optimal phase tracking electronically variable attenuators, and a compact high power limiter.

The focus of this review is the PIN diode model, PIN diode requirements, and other limiter and EVA design considerations that are impacted by PIN diode choice. Furthermore, the literature review discusses state of the art phase tracking EVAs.

Fig. 2.1 shows the literature review's layout.

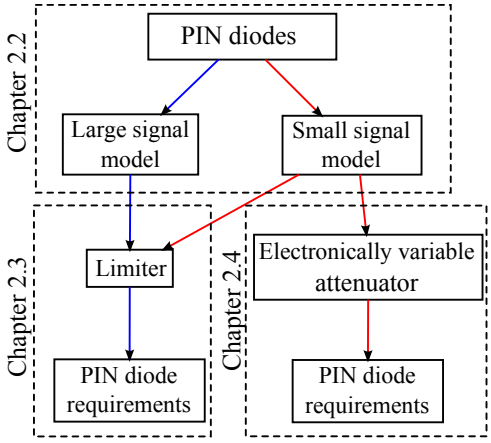

Figure 2.1: A diagram of the literature review, indicating how the different elements interact.

The physical properties of PIN diodes are reviewed in Section 2.2. PIN diodes are simulated with a small signal or large signal model, depending on the application. The small signal model is used in EVAs to calculate attenuation, while the large signal model is used to simulate switching behaviour in limiters.

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Typical designs for PIN diode limiters and PIN diode electronically variable attenuators are widely available [2], [1].

Section 2.3 gives an overview of limiters as receiver protectors. The limiter design process is summarised; this includes configurations, expected isolation and limitations brought on by PIN diode selection.

Designing a high power limiter for microstrip application has its own challenges, examined in Section 2.3.

Finally, available matched EVA topologies are given in Section 2.4, followed by PIN diode requirements. Current literature on EVA transmission phase response is also discussed.

2.2 PIN diodes

PIN diodes dictate many of the characteristics of limiters (e.g. transients, power handling) and EVAs (e.g. transmission magnitude and phase).

Section 2.2.1 gives the physical properties governing the behaviour of PIN diodes. From these attributes the small signal and large signal PIN diode models are found.

The PIN diode acts as a current controlled resistor at high frequencies, but its impedance is not purely resistive. The small signal model discussed in Section 2.2.2 shows the complex PIN diode impedance that affects transmission phase and attenuation of an EVA.

To simulate the PIN diode's transient response, a large signal model is needed. Caverly's PIN diode model is discussed in Section 2.2.3.

2.2.1 Physical properties of PIN diodes

PIN diodes consist of an intrinsic layer (I) of semiconductor wedged between highly doped P type and N type materials. By doping the N and P layers, the materials' resistivity decreases. Intrinsic silicon contains very little impurities (dopants), as a result it has a high resistivity [5].

When a PIN diode is forward biased, electrons and holes are injected into the I region. The injected charge carriers reach an equilibrium state. The increased charge carrier concentration in the I region lowers its resistivity and a conductive path forms through the I region. There is a finite time the charge carriers can exist in the I region before recombining. This average recombination time is known as the carrier lifetime (τ_L). Injecting more or fewer carriers into the I layer to increase or decrease its conductivity results in conductivity modulation [5].

Charge carriers can be injected into the I region through either an AC or a DC forward bias. For a time varying AC forward bias ($i_f(t)$), the charge in

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the I region is controlled by:

$$\frac{dq_s}{dt} = i_f(t) - \frac{q_s}{\tau_L} \tag{2.2.1}$$

If an RF signal is incident on the PIN diode, its positive cycle will inject carriers into the I region, forward biasing the PIN diode. Furthermore, above a lower frequency limit f_T the brief negative half cycle of the RF signal is not sufficient to remove all the charge in the I region. As a result, the PIN diode's impedance remains low.

It has already been stated that the PIN diode is a current controlled resistor at high frequencies. The lower frequency limit of the PIN diode's variable resistance operation is found where the RF period becomes comparable to the transit time of electrons and holes across the I region. An estimate of the lower cut off frequency is given by [6]:

$$f_T = \frac{1300}{w^2} \qquad \text{MHz} \tag{2.2.2}$$

where w is the I region width in microns.

When a DC current is applied, the equation for stored charge (Q_s) in the I region becomes:

$$Q_s = I_f \tau_L \tag{2.2.3}$$

Through analysis of the stored charge, average electron and hole density ($\overline{\mu} = \frac{\mu_e + \mu_p}{2}$) and the PIN diode area, the I region's resistivity is calculated as:

$$R_d = \frac{W_I^2}{2 I_f \overline{\mu} \tau_L} \tag{2.2.4}$$

where W_I is the I region width. A full derivation is found in [7]. R_d is not inversely proportional to I_f as implied by Eq. 2.2.4, since τ_L is current and temperature dependent [5].

The PIN diode's off-state properties are considered next. Additional to the PIN diode's variable I region resistance, its I region also behaves as a low loss parallel plate capacitor, its capacitance is calculated using:

$$C_j = \frac{\epsilon A}{W_I} \tag{2.2.5}$$

where C_j is the junction capacitance, $\epsilon = \epsilon_0 \epsilon_r$ is dependent on the I region's dielectric material and A is the device area [5].

When no forward bias current is applied to the PIN diode (zero bias), some charge may still exist in the I region. The additional charge in the I region reduces its effective width. From Eq. 2.2.5, a smaller I region width results in a larger junction capacitance. As reverse bias is increased, C_j decreases in value until zero punchthrough is reached, after which it remains nearly constant for

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further reverse bias. Zero punchthrough is the state where all charge has been swept clear of the PIN diode's I region. Due to the low carrier density in the I region of a PIN diode, its depletion region is much wider than typical PN diodes. As a result, PIN diode punchthrough is reached for relatively low voltage.

PIN diodes have a reverse breakdown voltage (V_B) that is proportional to the I region width. When V_B is exceeded, the PIN diode will enter avalanche breakdown where the reverse current increases rapidly and can result in PIN diode failure [7].

2.2.2 Small signal model

The PIN diode small signal model describes the PIN diode's linear behaviour. From the physical description in the previous section, some information about the PIN model is known:

- The P and N regions have a small resistance in series with the I region, R_s. In EVA applications, this resistance can be ignored since it is typically masked by the series inductance. In limiter applications, this is a critical value and should be included in the model.
- The I region has a large resistance that can be changed by forward biasing the PIN diode, R_d.
- There is a small capacitance in parallel with the I region resistance, called the junction capacitance, C_j.

Additional impedances that are present in a packaged PIN diode:

- There is a series inductance due to bond wire connections, L_s.
- Typically, a parallel package capacitance, C_{pkg}.

In the case of package parasitics, it will mostly depend on the type of package used. An application note describing different package parasitics is found in [8].

The small signal PIN diode model is shown in Fig. 2.2 [5]. Ideally, the P and N region resistances are small enough to be ignored when simulating EVAs. However, these resistances become extremely important when determining a limiter's power handling.

For large values of R_d, the junction capacitance dominates the PIN diode's equivalent impedance.

For small values of R_d, the junction capacitance has little effect, but the bond wire inductance and minimum resistance ($R_s + R_d$) will limit the smallest impedance the PIN diode can have.

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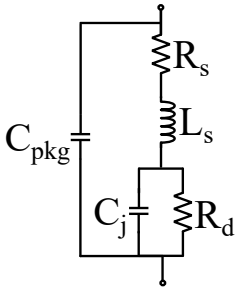

Figure 2.2: Small signal packaged PIN diode model.

The equivalent impedance of the small signal PIN diode is written as:

$$Z_{PIN} = R_s + \frac{R_d}{1 + (\omega C_j R_d)^2} + j(\omega L_s - \frac{\omega C_j R_d^2}{1 + (\omega C_j R_d)^2}) \tag{2.2.6}$$

when $C_{pkg} \approx 0$.

2.2.3 Large signal model

In limiter aplications the transient properties of PIN diodes are important. Caverly [9] proposed a large signal model that quite accurately describes the transient properties of the PIN diode.

The PIN diode's switching behaviour is controlled by the charge distribution in the I region. The model proposed by Caverly includes junction effects as well as low and high frequency I region charge storage and current dependent lifetime effects. This means that the PIN diode can be DC biased in the simulation and the results would be an accurate description of real world PIN diode behaviour.

The Caverly model includes the charge storage phenomenon in the I region by solving the charge density ($n(x,t)$) differential equation [9]:

$$\frac{\partial^2 n(x,t)}{dx^2} = \frac{n(x,t)}{D_a \tau} + \frac{1}{D_a}\frac{\partial n(x,t)}{dt} \tag{2.2.7}$$

where x is the length of the I region from the P-I junction to the I-N junction, D_a is the ambipolar diffusion constant and τ is the carrier lifetime. The solution is derived in [9], [10]. The result is an equation describing an RC type network that can be used to approximate the charge storage phenomenon in the I region.

The complete PIN diode large signal model is shown in Fig. 2.3. The junction behaviour is defined by sections (b) and (c) in Fig. 2.3, where the P-I and I-N junctions are represented by regular PN diode models. Section (a) of Fig. 2.3 represents the PIN diode's small signal behaviour with the addition of current controlled junction characteristics.

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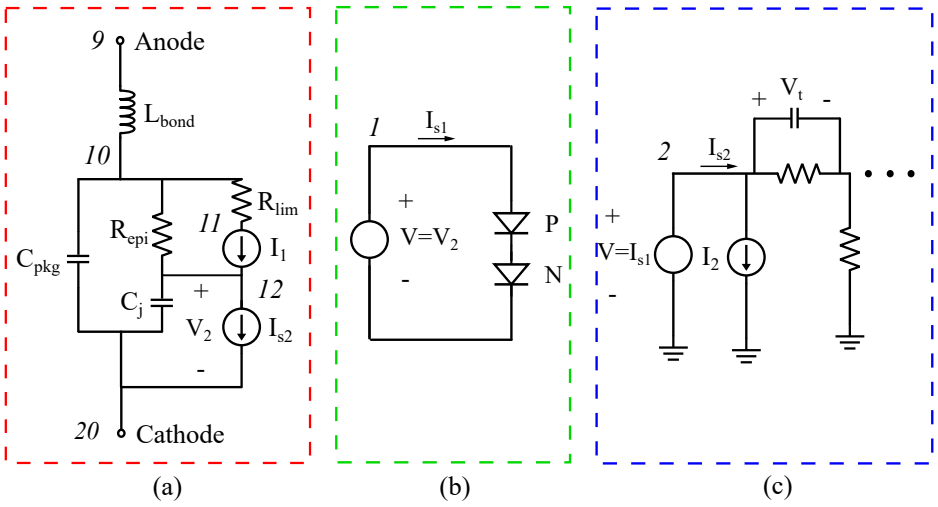

Figure 2.3: Full Caverly PIN diode model.

The section between nodes 10 and 12 in Fig. 2.3 accounts for the voltage drop on the base region of the PIN diode [11], where the controlled current source I_1 models the conductivity modulation. The current source I_2 at node 2 provides the emitter recombination effect. I_{s2} models and injects the current flowing through the diode into the cathode of the PIN diode model. The Caverly model is applied in programs such as *AWR Microwave Office*, Keysight's *Advanced Design System*, and *LTspice*. The *LTspice* Caverly model is given in Appendix A.

2.3 Limiters

Limiters are used as receiver protectors in radio and radar receiver applications [2]. The function of a receiver protector is to pass signals below some power threshold through with minimum insertion loss while attenuating signals above the power threshold.

Fig. 2.4 shows the layout of this section's limiter literature review. Additionally, this diagram summarises the design process of a limiter that is followed in this dissertation.

Receiver protectors are outlined in Section 2.3.1, where different configurations are described.

Section 2.3.2 discusses a PIN diode limiter and the typical isolation that can be expected.

In Section 2.3.3, PIN diode parameters that affect limiter operation are given.

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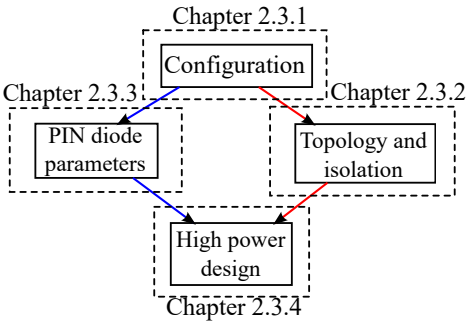

Figure 2.4: Layout of limiter literature review. The directions indicated also show the order wherein a limiter is designed in this dissertation.

Implementing a high power limiter on microstrip requires careful substrate and PIN diode heat transfer design, discussed in Section 2.3.4.

2.3.1 Receiver protectors

A receiver protector has two operating states: the blocking state where it attenuates (blocks) a damaging input signal, and the passing state where only a small portion of a target return signal is lost. The amount of protection provided by the receiver protector is the 'isolation'. When a receiver protector is in its passing state, the small signal loss is referred to as the 'insertion loss' [12].

There are three receiver protector configurations discussed here: passive, active and quasi-active [13]. A comparison of the three configurations is given in Table 2.1.

When an active limiter configuration is used for pulsed applications, a 'driver' delivers a fast bias current injection to the limiter at the pulse's leading edge. In some cases a driver also provides a reverse bias spike at the trailing edge of the pulse, improving the limiter's reverse recovery time.

A passive limiter has poor reverse recovery time, while an active limiter adds complexity and leaves the receiver unprotected from non-synchronous signals.

The quasi-active configuration is a good compromise in an active pulsed radar system.

The PIN diode limiter is one of several receiver protector technologies, including TR tube, Pre-TR tube and ferrite limiters. Due to advances in PIN diodes, the diode limiter has become an increasingly desirable option as a receiver protector [14].

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Table 2.1: Comparing performance of receiver protector architectures.

Architecture	Advantage	Disadvantage
Passive	Limits large in-band incident signals. The receiver is always protected, even when the radar is off. No power supplies required. No driver required.	Reverse recovery time is slow. Need reverse DC bias to improve insertion loss and recovery time.
Active	Limits synchronous RF signals. Low loss. Low leakage spikes. Faster recovery time.	No non-synchronous protection. DC power supplies required. Physical size. If the control signal fails,the receiver protector fails.
Quasi-active	Limits both synchronous and non synchronous signals. Low loss. Low leakage spikes. Provides protection when power is off.	Physical size. DC power supplies required.

2.3.2 PIN diode limiter

Fig. 2.5 shows a basic passive limiter configuration: a PIN diode connected in parallel with a load. When a large signal is incident on the PIN diode, the RF choke allows rectified current to flow through the diode. The rectified current passively forward biases the PIN diode, lowering its resistance. A forward

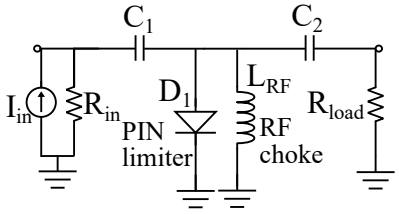

Figure 2.5: Circuit diagram of a simple limiter configuration.

biased PIN diode causes an impedance mismatch that reflects the incident signal.

PIN diodes can be AC or DC biased. Leenov [15] showed that a DC biased PIN diode provides significantly more isolation at high input power than a passively AC biased PIN diode.

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A limiter's isolation can be increased by about 6 dB for each PIN diode added in parallel. However, isolation in dB is approximately doubled when a PIN diode is added a quarter-wavelength away.

A shunt PIN diode has a convenient heat removal path to ground (or to a heat sink). For this reason all the considered limiter topologies will contain PIN diodes connected to ground.

2.3.2.1 Typical isolation

A single shunt PIN diode limiter provides isolation according to the equation [16]:

$$\text{Isolation} = 20\log\left(\frac{Z_0}{2R_d} + 1\right)\ dB \tag{2.3.1}$$

assuming the series inductance $L_s = 0$, and $Z_0 = R_{in} = R_{load}$. A single stage limiter can typically provide 20 to 30 dB of isolation depending on the operating frequency and PIN diode characteristics [2]. To achieve more isolation, consider the limiter with two PIN diodes separated by a quarter-wavelength transmission line in Fig. 2.6.

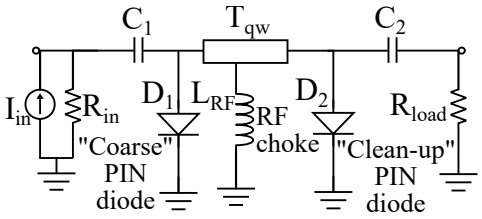

Figure 2.6: Two stage passive limiter, the first PIN diode limits most of the power while the second PIN diode determines the spike leakage and flat leakage (output power). T_{qw} is a quarter-wavelength transmission line at f_0 with a 50 Ω characteristic impedance.

The two stage limiter in Fig. 2.6 has a maximum isolation of:

$$\text{Isolation} = 20\log\left(\frac{(R_d + Z_0)^2 + R_d^2}{2R_d^2}\right)\ dB \tag{2.3.2}$$

when $L_s = 0$.

In a two stage limiter, the second PIN diode is referred to as the 'clean up stage', since it reduces the spike leakage and determines the flat leakage of the limiter [2]. These terms are discussed in the next section.

The second diode typically has a smaller I region width so its threshold level is low enough to provide sufficient protection to components further down the receiver chain. A PIN diode's threshold level is linearly proportional to its I region width. The narrower the I region, the lower the PIN diode's threshold level will be. The threshold level is also discussed in the next section.

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A smaller I region width typically indicates the PIN diode has a faster turn on time. When a large signal is incident on the limiter, the first diode does not switch on immediately and the signal travels to the second PIN diode which is chosen to have a faster switch on time. The changing impedance of the second PIN diode causes a standing wave on the quarter-wavelength line with a maximum at the first diode. This large voltage forces charge carriers through the first PIN diode and its impedance lowers faster than in the single diode case [2].

2.3.3 PIN diode limiter parameters

The following parameters determine the attributes of a limiter. The parameters are described with respect to a passive single PIN diode limiter as shown in Fig. 2.5.

2.3.3.1 Threshold level

The threshold level is the input power level at which the limiter's output is 1 dB below the expected value. This is also known as the 1 dB compression point of the output [2]. The I layer thickness is directly proportional to the PIN diode's threshold level.

When a PIN diode has an I layer of 1 μm the threshold level is $7-10$ dBm. With an I layer thickness of $7-10$ μm, the threshold level is $20-23$ dBm [2].

The threshold level can be decreased in a passive limiter by using a Schottky diode instead of an RF choke in antiparallel configuration with the PIN diode as in Fig. 2.7. The Schottky diode conducts at a lower threshold level, biasing

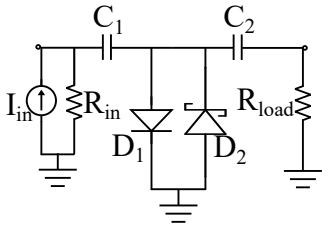

Figure 2.7: Single stage PIN diode (D_1) limiter with an anti-parallel connected Schottky diode (D_2) to lower the limiter's threshold.

the PIN diode before its own threshold is reached [17]. It is important to note that a Schottky diode severely increases the recovery time of the PIN diode limiter.

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2.3.3.2 Minority carrier lifetime (τ_L)

The minority carrier lifetime τ_L refers to the average time that charge carriers exist in the I region before the charge carriers are completely recombined [2]. For limiters this value has to be small since it determines the switch-off time [18]:

$$\tau_{FR} = \tau_L \log_e (1 + \frac{I_f}{I_R}) \tag{2.3.3}$$

where τ_{FR} is the time the diode takes to switch from forward to reverse bias, I_f is the forward current and I_R is the reverse current.

The minority carrier lifetime can be decreased for limiter PIN diodes by doping the intrinsic region with gold. However, gold doping increases the minimum resistance of the PIN diode [2]. A smaller equivalent PIN diode resistance results in less power dissipated in the diode, increasing the maximum input power that the PIN diode can handle.

2.3.3.3 Power handling

In its blocking state, the PIN diode is a small resistance (when $L_s = 0$) that causes an impedance mismatch with the input. Most of the incident power is reflected, only a small portion is dissipated in the PIN diode.

The power dissipated in a limiter is the sum of the DC and AC signals passing through the diode [2]:

$$P_d = I_{DC}V_{DC} + I_{RF}^2 R_p \approx I_{RF}^2 R_p \tag{2.3.4}$$

where I_{DC} and V_{DC} are the applied DC current and voltage, I_{RF} is the RF current due to the incident signal and $R_p = R_d + R_s$ is the total PIN diode resistance. The DC signals typically only dissipate a small amount of power and can be ignored [2]. Writing Eq. 2.3.4 in terms of the input power, the maximum power dissipated by a limiter PIN diode (P_d) is given by:

$$P_d = P_L \frac{4R_p}{Z_0} \tag{2.3.5}$$

where P_L is the input power and Z_0 is the characteristic impedance. The factor 4 in Eq. 2.3.5 comes from the line current doubling through the short circuit created by the forward biased PIN diode [16].

The maximum applied reverse voltage is limited by the breakdown voltage (V_B). The breakdown voltage is determined by the I region width of the PIN diode [7]. The maximum reverse voltage rating (V_B) of a PIN diode should not be exceeded [18].

2.3.3.4 Spike and flat leakage

During the PIN diode's turn on transient, it traverses its entire range of isolation. The power dissipated in the diode varies during this transition. A part

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of the RF energy leaks through in a pulse at the leading edge of the input signal, known as the spike leakage [5].

Fig. 2.8 shows the spike leakage of a power pulse, followed by the flat leakage. The PIN diode takes approximately the carrier transit time across

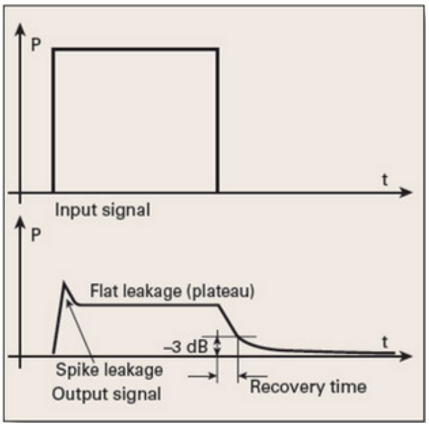

Figure 2.8: The spike and flat leakage of a transmitted power pulse [5].

the I region to reach its minimum resistance value, where the final isolation (flat leakage) of the minimum resistance is reached [2].

The isolation provided by the PIN diode is dependent on the input power. As the input power increases, the PIN diode's resistance decreases until it reaches its minimum value, known as its saturation resistance R_{sat}. When R_{sat} is reached the output power increases again dB per dB with the input power [2].

2.3.3.5 Reverse recovery time

Reverse recovery describes the turn off transient of the PIN diode. When the PIN diode has to return to its zero bias state, there are still free charge carriers in the I region, keeping its resistance low [2]. The limiter now provides isolation when no more large signals are present. Consequently, any target signals incident on the receiver is attenuated. This temporarily degrades the sensitivity of the receiver [2].

Without an external bias current forcing the free charge carriers from the I region, the free charge carriers are eliminated through recombination. The recombination time is proportional to the minority carrier lifetime [2], as was shown in Eq. 2.3.3.

The switching time of a PIN diode can be improved by biasing it with a driver that has high values of reverse current, or that biases the PIN diode with a spiked leading edge [5].

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2.3.3.6 Schottky diodes

Using a Schottky diode in a passive limiter decreases the limiter's turn on time, it also reduces second harmonic distortion as discussed by Lim [17]. A drawback is that the addition of a Schottky diode increases the reverse recovery time of the PIN diode limiter.

A Schottky diode's reverse breakdown voltage is another limiting factor in the maximum input power that the limiter can handle.

A trade off to consider when using Schottky diodes in limiter design, is the Schottky diode's breakdown voltage and junction capacitance.

The small signal response of a limiter can be severely degraded by large parallel capacitance added by the PIN and Schottky diodes.

2.3.4 Microstrip high power design considerations

For high power operation, there are two power considerations that apply to the embedding circuitry: temperature increase due to average power dissipation, and voltage arcing because of peak power.

If a limiter is designed for microstrip, the loss in the conductor and the dielectric material of the substrate results in a temperature rise. The substrate's dielectric material and thickness have to be chosen to withstand a particular input power and the corresponding conductor temperature increase.

Power dissipated in the PIN diode causes a temperature increase in the PIN diode's junction. By constructing a thermal model of the PIN diode's junction, it is possible to estimate the total temperature increase at the junction.

Voltage arcing depends on the dielectric strength of the material the signal is propagating through. This section shows how to determine if voltage arcing is likely to happen in a particular microstrip limiter.

2.3.4.1 PIN diode heating

Junction heating limits the maximum average power that can be incident on a PIN diode. The majority of the power absorbed by a PIN diode is dissipated in the I and N layers [2].

In a PIN diode, heat flow through convection and radiation is negligible [2]. Additionally, the conduction of heat through the PIN diode's bond wires is small enough to be ignored [2]. Only heat conduction from the I layer to ambient is considered further.

To maintain safe operating conditions for a PIN diode, its maximum junction temperature should not be exceeded. Typical maximum junction temperatures range between 150 and 200 ^oC.

PIN diodes have a parameter called the continuous wave (CW) thermal resistance θ_{jc} in $^oC/W$ that indicates the temperature rise per Watt of power

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dissipated in the diode's junction:

$$T_j = T_{a/heatsink} + P_d\theta_{jc} \tag{2.3.6}$$

where T_j is the junction temperature, T_a is the ambient/heatsink temperature and P_d is the dissipated power.

For a CW signal, the temperature rise reaches an equilibrium indicated by the above equation. In pulsed applications the heating does not reach an equilibrium immediately, the diode is heated only for a portion of the duty cycle. Another parameter called the heat capacity (HC) becomes relevant.

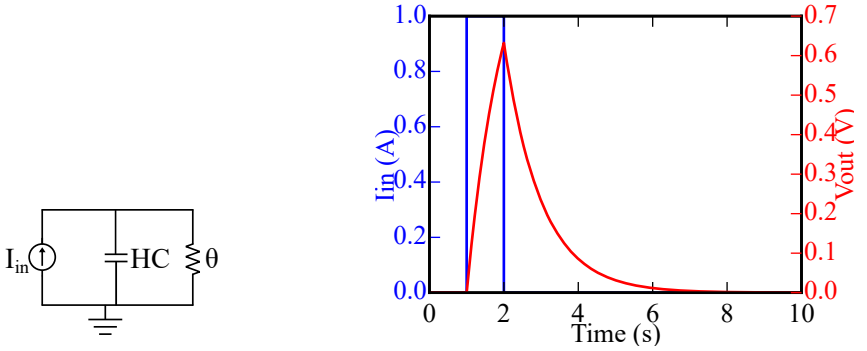
The heat capacity is analogous to a capacitor in an electric circuit, and the thermal resistance equates to a resistor in an electric circuit. Together, the heat capacity and thermal resistance creates a thermal time constant that dictates the time the PIN diode's junction takes to increase in temperature.

The thermal time constant determines the charge and discharge cycle of the temperature increase in pulsed applications:

$$\tau_{jc} = \theta_{jc}HC \tag{2.3.7}$$

where τ_{jc} is the thermal time constant of the PIN diode's junction.

Fig. 2.9a shows a circuit diagram consisting of a heat capacity (HC) and thermal resistance (θ). The current source represents the pulsed input power. Fig. 2.9b shows the temperature increase of the circuit in Fig. 2.9a when



(a) Circuit diagram. (b) Thermal time constant.

Figure 2.9: Circuit diagram analogy of a thermal resistance and heat capacity.

$HC = \theta = 1$ for a 1 W, 1 s pulse input.

The PIN diode only reaches its final temperature after approximately $6\tau_{th}$ has passed [19]. The delta temperature increase for a pulsed signal is given by [5]:

$$\Delta T_j = P_d\theta_j(1 - e^{\frac{-t}{\tau_{th}}}) \tag{2.3.8}$$

where τ_{th} is the thermal time constant of the entire circuit.

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To include heat conduction from the I region to ambient, a PIN diode's heat removal path is shown in Fig. 2.10. The model does not include solder joints or peripheral silicon.

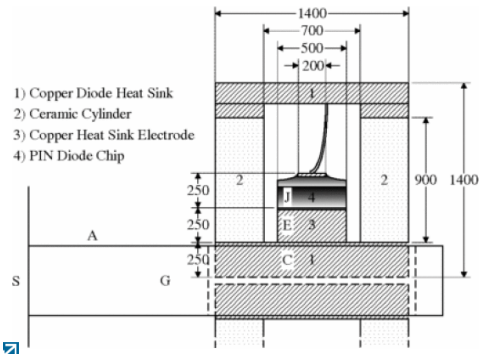

Figure 2.10: Constructional model of PIN diode's heat removal path [6].

A thermal equivalent circuit of Fig. 2.10 is given in Fig. 2.11 [6]. The capacitance C_{JE} ($C_{jc}/2$) is added to ensure correct average temperature within the PIN diode silicon [20]. The source current represents the average power dissipated in the PIN diode.

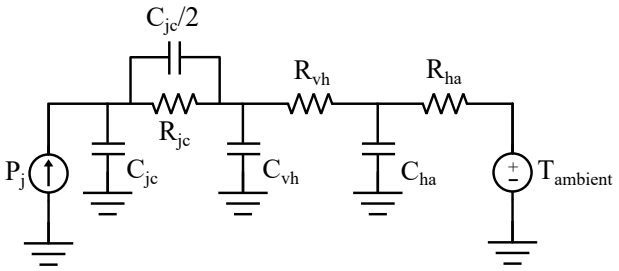

Figure 2.11: Thermal model of a PIN diode as proposed in [6], with the addition of C_{JE} as proposed in [20].

For pulsed applications, the heat capacities of the circuit has to be taken into account. In the case where the heat capacity is not given, it can be calculated using the object's physical dimensions. The thermal capacitance of an object with density ρ and volume V_b is given by [20], [6]:

$$HC = \rho c_\theta V_b \ \ J/^oC \tag{2.3.9}$$

where c_θ is the specific heat capacity of the material.

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Consider a rod with length l and area A where its ends are at thermal equilibrium. The steady state thermal resistance of this object can be calculated using Eq. 2.3.10 [6], where σ is the thermal conductivity of the material:

$$\theta_T \approx \frac{1}{\sigma}\frac{l}{A} \ ^oC/W \tag{2.3.10}$$

2.3.4.2 Microstrip substrate heating

Rogers Corporation [21] gives equations to estimate the temperature rise in a microstrip transmission line due to resistive heating. The following assumptions are made [21]:

- All heat generated by current or RF power is conducted from the point of generation only in the Z-direction to the ground plane(s).
- All the insertion loss of RF power is accounted for as heat generated in the conductor trace.
- A steady state has been reached.
- The heat generated is evident as a uniform temperature rise in the metal conductor and the ground plane(s) maintain(s) a uniform temperature.

The power dissipated in Watt over a length of line (L) is given by:

$$\begin{aligned} P_L &= P_I - P_T \\ &= P_I[1 - 10^{\frac{-\alpha L}{10}}] \end{aligned} \tag{2.3.11}$$

where P_I is the incident power and P_T is the transmitted power, α is the insertion loss in dB/m. The increase in temperature is determined by [21]:

$$\begin{aligned} \Delta T &= \frac{P_L H}{LWA} \\ &= \frac{HP_I[1 - 10^{\frac{-\alpha L}{10}}]}{LWA} \end{aligned} \tag{2.3.12}$$

where H is the dielectric thickness (m), W is the line width (m) and A is the thermal conductivity of the dielectric in W/mK. These equations do not take surface roughness into account. Surface roughness increases the loss in the conductor over frequency.

2.3.4.3 Peak power handling

The peak voltage that can be applied to a microstrip circuit without causing dielectric breakdown determines the peak power handling of the circuit.

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The peak power that a microstrip circuit can handle is given by [22]:

$$P_{pk} = \frac{V_{pk}^2}{2Z_0} \tag{2.3.13}$$

where V_{pk} is the maximum voltage and Z_0 is the characteristic impedance of the transmission line. The equation is valid for a matched circuit.

In circuits with a large voltage standing wave ratio (VSWR), the power handling is reduced by 6 dB. Given the input voltage, the maximum voltage in a circuit with a large VSWR is given by [23]:

$$V_{max} = V_{in}\frac{2\,VSWR}{VSWR+1} \approx 2V_{in} \tag{2.3.14}$$

The VSWR should be taken into account as a safety factor.

Voltage breakdown occurs when peak electric field of a material is reached, resulting in failure through arcing. When arcing occurs, a short circuit to ground is created in the material [24].

In general, the transition between the coaxial connector and the microstrip circuit will break down long before the microstrip line [22].

Peak electric breakdown field (E_{pk} given in V/m) for dry air at sea level is approximately 3 000 000 V/m [22], while the peak electric breakdown field of PTFE (Teflon) is 19 700 000 V/m [25].

The peak breakdown voltage of a coaxial connector can be calculated using [26]:

$$V_{pk} = E_{pk} a \ln\frac{b}{a} \tag{2.3.15}$$

where a is the radii of the inner conductor and b is the radii of the outer conductor in mm. When the coaxial connector transitions to air (and the microstrip), the greatest risk for reaching breakdown usually exists.

2.4 Electronically variable attenuators

Electronically variable attenuators (EVA) are used in receiver front ends for sensitivity time control (STC) [13]. Controlled attenuation over time improves the dynamic range of the receiver.

EVAs use PIN diodes as current controlled resistors. The output signal's level is varied by changing the forward current applied to the PIN diodes.

Fig. 2.12 shows the layout of the EVA literature section. It also indicates the initial design steps used in this dissertation to identify the most appropriate EVA for a multi-channel receiver.

The first step of EVA design is to establish the system's requirements:

1. A poor EVA reflection coefficient translates to a large portion of the input or output signal that is re-reflected from external circuitry. When

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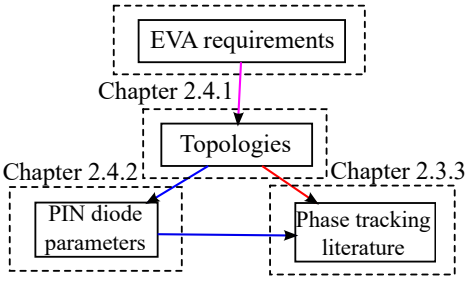

Figure 2.12: Layout of electronically variable attenuator literature section.

there are multiple channels in a receiver, the components in each channel will not have identical reflection coefficients due to component tolerances. Signals that are re-reflected from components that are not precisely matched in each channel results in phase tracking errors between channels.

2. The PIN diode impedance is dependent on biasing current. For multiple biasing schemes in a single EVA, the possibility for impedance mismatches between PIN diodes, and ultimately phase tracking errors increase.

The initial requirements of a set of EVAs used in a multi-channel reciever are:

1. Matched input and output ports.

2. Simple biasing scheme with a single current source.

Given the above criteria, a selection of EVAs from [1] is briefly discussed in Section 2.4.1. Their attenuation is given in terms of PIN diode resistance R_d.

Section 2.4.2 discusses PIN diode parameters that will affect an EVA's response.

Current literature contains many examples of improvements on classic attenuator topologies, Section 2.4.3 examines several EVAs in terms of improvements to their transmission phase response.

2.4.1 Electronically variable attenuator topologies

The EVA attenuation described in this section is given for the ideal case, when $L_s = 0$ and $C_j = 0$.

2.4.1.1 Quadrature hybrid attenuators

Two types of quadrature hybrid attenuators are shown in Figs. 2.13 and 2.14. The input signal is divided into equal in phase (I) and quadrature (Q) components where the I and Q channels are terminated in PIN diodes. The reflected

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signals are added constructively towards the hybrid coupler's fourth output port. The reflected signals cancel towards the hybrid coupler's input, allowing the input to be isolated from the mismatched reflections.

The series quadrature hybrid attenuator's PIN diodes are connected in series with a 50 Ω resistor, and its attenuation in the ideal case is given by [1]:

$$Att_{quadSeries} = 20\log\left(1 + \frac{2R_{50}}{R_d}\right)\ dB \tag{2.4.1}$$

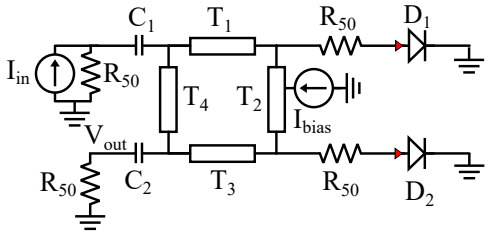

Figure 2.13: Quadrature hybrid attenuator with series connected PIN diodes. All transmission lines are a quarter-wavelength at the center frequency, T_1 and T_3 have a characteristic impedance of $\approx 35\ \Omega$ and T_2 and T_4 are 50 Ω.

The shunt quadrature hybrid attenuator's PIN diodes are connected in parallel with a 50 Ω resistor, and its attenuation is given by [1]:

$$Att_{quadShunt} = 20\log\left(1 + \frac{2R_d}{R_{50}}\right)\ dB \tag{2.4.2}$$

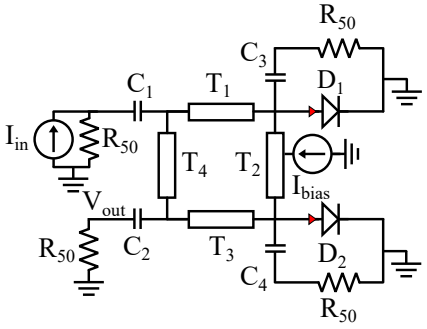

Figure 2.14: Quadrature hybrid attenuator with shunt connected PIN diodes. All transmission lines are a quarter-wavelength at the center frequency, T_1 and T_3 have a characteristic impedance of $\approx 35\ \Omega$ and T_2 and T_4 are 50 Ω.

Another microwave matched attenuator using a quadrature hybrid coupler is the double hybrid attenuator shown in Fig. 2.15 [27]. Once again the input

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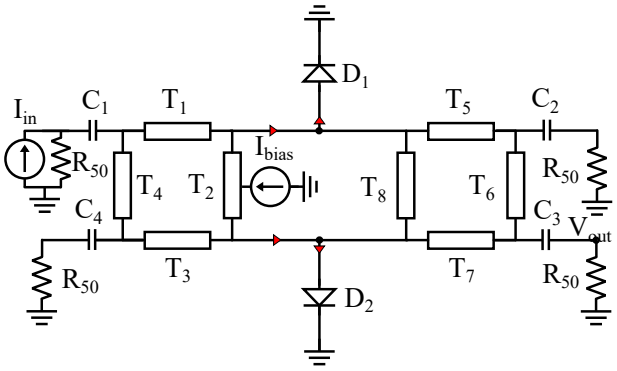

Figure 2.15: Double hybrid PIN diode attenuator with shunt connected PIN diodes. The quarter-wavelength (at the center frequency) transmission lines T_1, T_3, T_5 and T_7 have a characteristic impedance of $\approx 35\ \Omega$, while T_2, T_4, T_6 and T_8 are 50 Ω lines.

signal is divided into its I and Q components. Both I and Q signals are attenuated by shunt PIN diodes after which the attenuated I and Q signals are added constructively in a second hybrid coupler. The attenuation of the double hybrid attenuator is approximately the shunt PIN diode's attenuation [1]:

$$Att_{doubleHybrid} = 20\log\left(1 + \frac{Z_0}{2R_d}\right)\ dB \tag{2.4.3}$$

2.4.1.2 Quarter-wave attenuators

Quarter-wave line sections are used to create matched attenuators [1]. A series quarter-wave attenuator is shown in Fig. 2.16, and a parallel quarter-wave attenuator is given in Fig. 2.17.

The series quarter-wave attenuator looks similar to two parallel PIN diodes separated by a quarter-wavelength (at the center frequency) transmission line. However, by adding a resistor with an impedance of $R_{50} = 50\ \Omega$ in series with the first PIN diode, the series quarter-wave configuration can have a matched input over its full control range. The series resistor R_{50} reduces the maximum attenuation that can be achieved by keeping the equivalent impedance above 50 Ω at the input. The output PIN diode is free to vary over its entire resistance range. The output will not be matched when PIN diode D_2's equivalent resistance is small.

The attenuation performance of the series connected quarter-wave attenuator is given by [1]:

$$Att_{quartSeries} = 20\log\left(1 + \frac{R_{50}}{R_d}\right)\ dB \tag{2.4.4}$$

The parallel connected quarter-wave attenuator has a PIN diode in parallel with R_{50}, which is then transformed through a quarter-wavelength line to the

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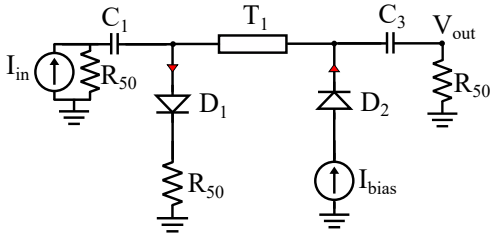

Figure 2.16: Series connected quarter-wave attenuator. Transmission line T_1 is a quarter-wavelength at the center frequency with a characteristic impedance of 50 Ω.

input. The equivalent impedance of the PIN diode and $R_{50} = 50\ \Omega$ will always be below 50 Ω, but it is transformed through the quarter-wave line to be a large impedance at the input of the attenuator. When the PIN diode resistance is small, the impedance looking into T_1 from the junction with C_1 is large. The equivalent impedance seen by the input is nearly 50 Ω for a small PIN diode resistance. The result is a matched input, while the output of the attenuator is not matched.

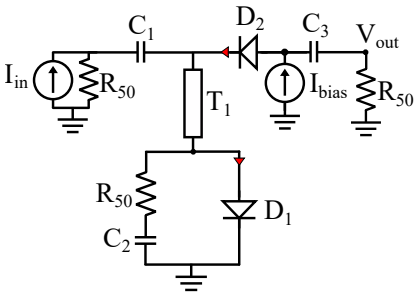

Figure 2.17: Parallel connected quarter-wave attenuator. Transmission line T_1 is a quarter-wavelength at the center frequency with a characteristic impedance of 50 Ω.

The attenuation performance of the parallel quarter-wave attenuator is given by [1]:

$$Att_{quartParallel} = 20\log\left(1 + \frac{R_d}{R_{50}}\right)\ dB \tag{2.4.5}$$

A drawback of the series and parallel quarter-wave attenuators is that they are only matched at the input port.

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2.4.2 PIN diode requirements

2.4.2.1 I region width

A PIN diode with a wider I region width will have less distortion in its forward biased operation than a PIN diode with a thinner I region [28]. Conversely, a wider I region instead of a thinner I region results in more distortion when a PIN diode is reverse biased.

2.4.2.2 Transmission response tracking in a set of EVAs

In [5], it is stated that an EVA implemented in a receiver front end requires repeatable performance in a set of EVAs. The EVA's response tracking in a set of EVAs is dependent on the PIN diode's complex impedance tolerance, as well as other component tolerances.

In [29] there is mention of the double hybrid attenuator's good repeatability. However, there is no comparison to other attenuators' repeatability or a method to determine the repeatability other than building and measuring multiple circuits.

2.4.2.3 Complex PIN diode impedance

If the complex part of the PIN diode impedance is disregarded, the PIN diode's resistance range determines the attenuation range. This can be seen from Eq. 2.4.1 to Eq. 2.4.5.

Bond wire inductance adds a reactance in series with the PIN diode resistance that limits the minimum impedance of the PIN diode. The junction capacitance limits the PIN diode's maximum impedance. As a result, an EVA's attenuation range is limited by the equivalent complex impedance of the PIN diode that is used.

The complex part of a PIN diode impedance can be compensated for in certain cases by careful transmission line design [5], [30], [31].

The complex PIN diode impedance causes the transmission phase to change from the ideal case. As the PIN diode resistance changes over its full control range, its effect on the phase response also changes.

2.4.3 Performance of electronically variable attenuators in the literature

The complex PIN diode impedance changes the EVA's transmission phase over PIN diode control range. Many improvements with regard to impedance compensation has been proposed. However, these improvements do not consider the tolerance error effect within a set of EVAs. An overview of EVAs found in current publications is given, with reference to the transmission phase improvement they provide.

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2.4.3.1 Low phase deviation between attenuation levels

Walker [32] analysed the parallel quarter-wave attenuator in Fig. 2.18 and proposed a phase correction equation. This entails adjusting the length of the

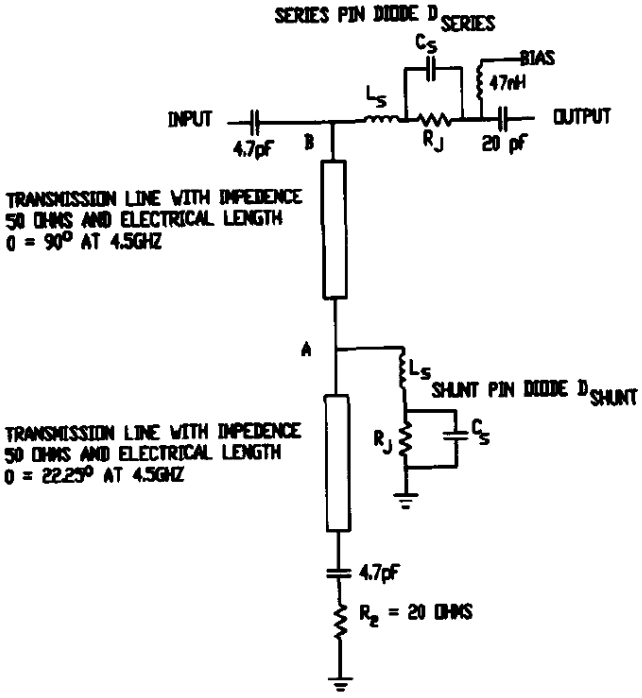

Figure 2.18: Parallel quarter-wave attenuator proposed by Walker [32].

transmission lines to compensate for the complex impedance of the PIN diodes in the attenuator. The overall goal of these corrections is to reduce the phase variation between attenuation levels. This is not the same as phase tracking within a set of attenuators.

Walker [32] proposed a back to back configuration of the parallel quarter-wave attenuator to improve its output match. However, in the article no further circuit diagrams or analysis is presented.

A United States patent was filed in 2007 detailing the design of Walker's proposed attenuator, the circuit is given in Fig. 2.19.

Fig. 2.19 shows a back to back connected parallel quarter-wave attenuator separated by a quarter-wavelength line [33]. The quarter-wave line connecting the two back to back parallel quarter-wave attenuators is divided by an inductor to ground, serving as a DC path to ground for both attenuators' biasing schemes.

A dual biasing supply applied in Fig. 2.19 through inductors L_2 and L_8 is used to provide equal current to all the PIN diodes, subsequently increasing possible variations between PIN diode impedances.

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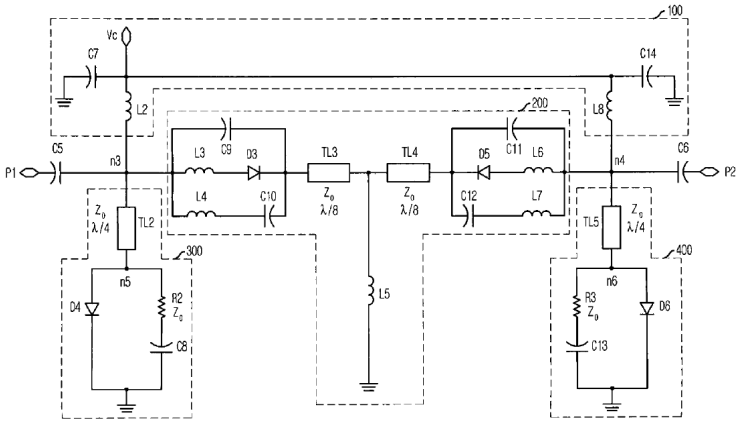

Figure 2.19: Back to back connected parallel quarter-wave attenuator separated by a quarter-wavelength line [33].

This topology has a much larger attenuation range but no further mention is made of the topology's phase response or phase deviation between attenuation states.

2.4.3.2 Shunt PIN diode attenuators with minimised phase shift

In [30], a three PIN diode shunt attenuator is proposed where the PIN diode complex impedance is embedded in low pass filters. The circuit is shown in Fig. 2.20.

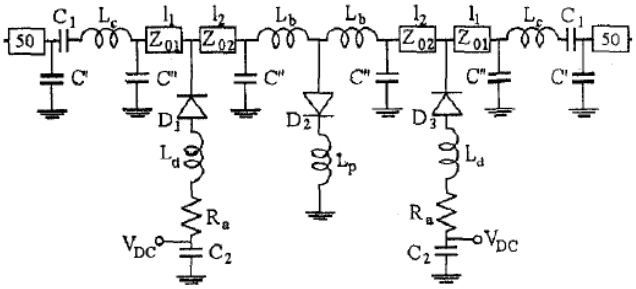

Figure 2.20: Three PIN diode shunt attenuator is proposed where the PIN diode complex impedance is embedded in low pass filters [30].

The attenuation flatness is insufficient for attenuation levels of more than 20 dB. This type of attenuator is also not matched over its entire attenuation range.

If the PIN diodes are correctly selected, this type of attenuator offers less distortion for medium and high input powers [30].

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Another shunt connected PIN diode attenuator in [31], given in Fig. 2.21, uses transmission lines between PIN diodes to compensate for PIN diode complex impedance and minimise the phase shift through the attenuator.

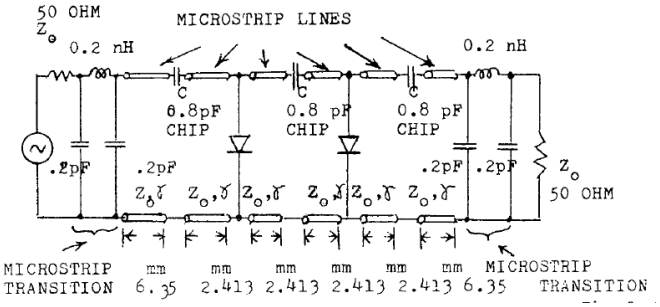

Figure 2.21: Transmission line compensation for PIN diode complex impedance [31].

2.4.3.3 Tuning out PIN diode parasitics

For a bandwidth between 1.91 - 2.01 GHz, the hybrid attenuator in [34] has a dynamic range of 14 dB with an attenuation flatness of 0.02 dB, and a phase change of 0.2 $^o/dB$ over the entire range. This topology shown in Fig. 2.22

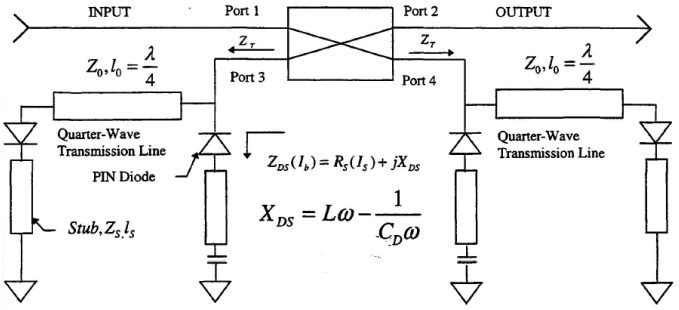

Figure 2.22: Hybrid attenuator with quarter-wave stubs to tune out PIN diode complex impedance [34].

uses quarter-wave stubs to tune out the PIN diode's complex component. The quarter-wave stubs together with the already large structure of the hybrid coupler results in an unacceptably large layout. Another drawback is that the dynamic range of the attenuator is limited.

A quadrature hybrid attenuator in [35] uses a transmission line to compensate for PIN diode parasitics at X-band. The attenuator's attenuation range is from 1.5 to 20 dB. The hybrid attenuator in [35] has an input and output reflection coefficient of better than -20 dB over its band of operation.

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Finally, the double hybrid attenuator is also discussed with reference to its transmission phase characteristics. The concept of using two hybrid couplers to form a double hybrid attenuator was first discussed in [36].

In [27], matching stub sections are used to compensate for PIN diode complex impedance. Fig. 2.23 shows a circuit diagram of the double hybrid attenuator from [27].

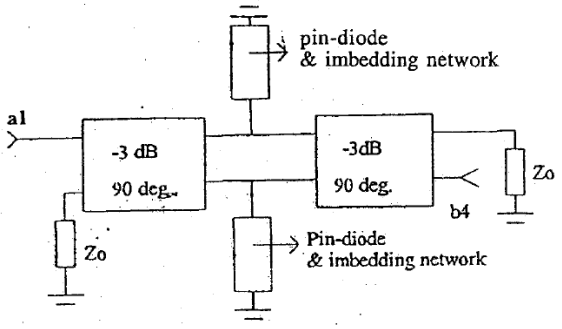

Figure 2.23: Double hybrid attenuator using stub sections to compensate for complex PIN diode impedance [27].

The double hybrid attenuator in [27] has an attenuation range between 2.5 and 19 dB with its center frequency at 2.4 GHz.

An improvement on the bandwidth performance of the double hybrid attenuator is presented in [37], where a 0 dB branchline coupler is used.

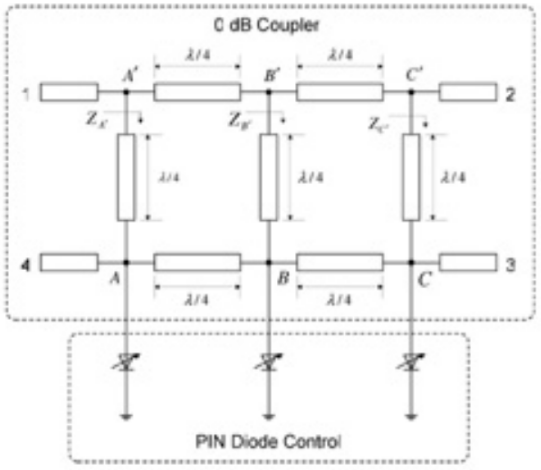

Figure 2.24: 0 dB Branchline coupler [37].

The 0 dB branchline attenuator in Fig. 2.24 has an attenuation range between 0.7 and 23 dB with its center frequency at 1.9 GHz.

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Both the double hybrid and 0 dB branchline attenuators have good input and output reflection coefficients. No attention was given to the transmission phase characteristics of the 0 dB branchline attenuator.

2.5 Conclusion

The dissertation has two distinct goals. To develop a set of optimal phase tracking EVAs, and develop and characterise a high power compact limiter that offers both active and passive protection to a multi-channel receiver.

PIN diodes are used as current controlled resistors in both limiters and EVAs. Variations in PIN diode complex impedance cause transmission phase variations within a set of EVAs over control range.

In Section 2.2, the PIN diode was described in terms of its physical properties. Using the discussed physical properties, a PIN diode's small signal and large signal simulation models were given.

Limiters are used in receivers to isolate sensitive components from large damaging signals. The multiple design choices for limiter development was given in Section 2.3.

EVAs were discussed in Section 2.4 in terms of their attenuation performance. A comprehensive review of EVA articles relating to phase response was examined. There were many suggested improvements to the change in transmission phase in [32], [38], [31]. However, none of the EVAs found in the literature discussed the transmission phase tracking performance within a set of attenuators.

Poor phase tracking between channels due to component and manufacturing tolerances could cause a detection error in the direction of arrival estimation in multi-channel radar. A method of analysing different EVA topologies and identifying a set of optimal phase tracking networks is needed.

The expected RMS phase error due to component tolerances can be found with sensitivity analysis. No references were found in the literature where the output response of PIN diode EVAs were analysed and compared using sensitivity analysis with the specific goal of ranking phase tracking performance of a set of attenuators.

The information provided in the literature study will be used to develop a limiter and EVA. The phase tracking condition still has to be met. A comprehensive description of sensitivity analysis is given in Chapter 3.

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Chapter 3

Sensitivity Analysis of Lumped and Distributed Linear Networks

3.1 Introduction

Multi-channel receivers often require good transmission phase tracking between channels. Tolerances in a network's lumped and distributed element values cause phase tracking errors within a set of networks. This raises the question: for a set of EVAs, is there a topology that will have optimal phase tracking within its multi-channel set?

Frequency domain sensitivity analysis quantifies the relative change in a complex valued output due to small relative changes in component values. In this chapter, output sensitivities with respect to variations in lumped and distributed elements are derived. The solution of a linear network's sensitivities is found here by mathematical manipulation of the output variable without reference to an adjoint circuit. Interpretation of the output sensitivities is explained with an example.

A frequency domain network model consisting of source currents, node voltages and branch admittances is developed in Section 3.2. Traditionally, Tellegen's theorem [39] is used to determine a circuit's sensitivity making use of an adjoint circuit. In Section 3.3 an alternative mathematical method is developed.

Sensitivity analysis is performed on network output voltages derived through nodal analysis, resulting in an output magnitude and phase sensitivity with respect to each circuit component. If the network is large, there will be many calculated sensitivities. A single comparable measure is needed to examine the effect of component tolerances on the transmission phase of a network. To find a single measure to compare networks in terms of their phase tracking, a root sum square (RSS) error measure is derived in Section 3.3.2.

In this chapter, a tool is developed that is used to solve the output sensitivities of linear networks consisting of lumped and distributed components.

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Valuable insight is gained from calculating the multiple output sensitivities due to component tolerances of a network.

By using sensitivity analysis and the application specific RSS error measure, the expected RMS phase error due to component tolerances is predicted. An optimal phase tracking topology is identified through this analysis by comparing the output RSS error measure of several networks.

3.2 Nodal analysis

The application of sensitivity analysis to the frequency domain nodal voltages of a linear network has been well documented [4], [40], [22]. By solving the frequency domain nodal voltages of a network, the network's transmission phase is found.

From [22], it is known that the characteristic impedance of a transmission line varies according to transmission line dimensional tolerances. In this chapter, transmission line variations are also included in a larger analysis to calculate the output voltage sensitivity to transmission line dimensional tolerances. Deriving the nodal voltage equations for networks that contain transmission lines become increasingly complex; their admittance matrices can not be reliably found through inspection.

As part of this dissertation, a circuit simulator is created that takes a linear circuit netlist as its input and solves the network's output voltages and output sensitivities. Section 3.2.1 briefly reviews network topology, from which the incidence matrix arises. Section 3.2.2 shows how the incidence matrix is used in nodal analysis. This is a useful tool to automate nodal analysis, while simultaneously simplifying the solution of output sensitivities. The *Python* code used to solve network sensitivities is given in Appendix B.

3.2.1 Directed graphs and the incidence matrix

A lumped network obeys three laws: Kirchhoff's Current Law (KCL), Kirchhoff's Voltage Law (KVL) and the elements' branch characteristics [41]. The branch characteristics give information on branch interconnections, as well as current flow direction.

Network topology describes a network's element properties and branch interconnections [41].

Branch connections, branch currents and branch voltages are depicted by drawing a directed graph [41]. As an example, consider the series quarter-wave attenuator in Fig. 3.1a, where R_{50} is a fixed 50 Ω resistor, R_{d1} and R_{d2} are variable resistors and T_1 is a quarter-wavelength, 50 Ω transmission line. A directed graph is drawn by replacing each circuit element with a line segment as in Fig. 3.1b. Each *branch* is indicated by a letter from a to g, the *nodes* are numbered 1 to 4. Current direction is indicated on each branch in Fig. 3.1b.

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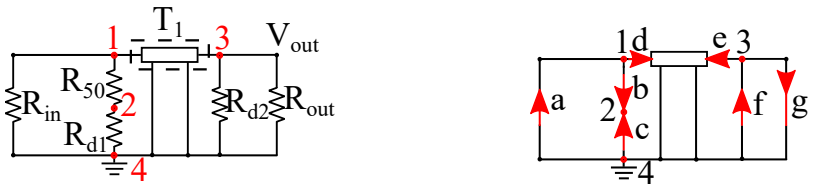
Branch voltage is defined with its positive terminal at the origin of the current flow direction.



(a) Circuit diagram. (b) Directed graph.

Figure 3.1: Lumped element network with transmission line and its derived directed graph.

The incidence matrix is created by taking the information found in a directed graph and placing it in a matrix. The rows in an incidence matrix represent the n nodes in a lumped element network, while the columns denote the z branches.

A formal definition of a node-branch incidence matrix as formulated in Chua and Lin [41] is:

For a directed graph G_d with n nodes (excluding the reference node) and z branches, we define the incidence matrix to be an $(n + 1)$ x z matrix (including the reference node)

$$\mathbf{A}_a = [a_{ij}]$$

where

$a_{ij} = 1$ if branch j is incident at node i, and the arrow is pointing away from node i

$a_{ij} = -1$ if branch j is incident at node i, and the arrow is pointing toward node i

$a_{ij} = 0$ if branch j is not incident at node i

Using the above definition, the incidence matrix of the directed graph in Fig. 3.1b is:

$$\mathbf{A}_a = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \end{array} \begin{array}{c} \begin{array}{ccccccc} a & b & c & d & e & f & g \end{array} \\ \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 1 \\ 1 & 0 & -1 & -1 & -1 & 1 & -1 \end{bmatrix} \end{array}$$

Every branch of a network connects to two nodes, consequently every column in the matrix has two nonzero elements, a 1 and a -1. This is stated mathematically by defining a z x 1 columm vector containing the branch currents $\mathbf{I}_b$, thus [41]:

$$\mathbf{A}_a \mathbf{I}_b = \mathbf{0} \tag{3.2.1}$$

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It is possible to delete any one row in $\mathbf{A}_a$ without losing any information, since the deleted row can be returned any time by following the rule that every column has to add up to zero [41]. The deleted row is referred to as the datum node, or the circuit's ground reference, indicated in Fig. 3.1b as node 4. The reduced incidence matrix will be referred to as $\mathbf{A}$. By deleting any one of the rows in $\mathbf{A}_a$, the remaining n equations are linearly independent. In network analysis we need independent equations [41].

3.2.2 Circuit analysis using the incidence matrix

The incidence matrix greatly simplifies circuit analysis of a large network. By using the incidence matrix, a linear network's steady state solution is derived through a set of nodal equations that contain complex valued voltages (V), currents (I) and admittances (Y) [41].

To aid in the derivation of an arbitrary network's incidence matrix, the lumped and distributed elements are modelled as two port devices defined by specific element characteristics (values). The input and output ports are represented by the branches at the input and output of the element in the directed graph [42]. The characteristic value of each element in a network is placed in a z x z branch admittance matrix $\mathbf{Y}_z$, where z is the number of branches in the network. The lumped elements are placed on the diagonal in the branch admittance matrix according to [41]:

$$Y_{mn} = \begin{cases} 0, & n \neq m \\ \frac{1}{Z_{mm}}, & n = m \end{cases} \tag{3.2.2}$$

where Z_{mm} is the impedance of any linear resistor, inductor or capacitor, and m and n are the entrance and exit branches of the current element. A distributed element transmission line's two port Y parameters are added to the branch admittance matrix as [43]:

$$Y_{mn} = \begin{cases} \frac{j}{Z_0 \sin \beta l}, & n \neq m \\ \frac{1}{jZ_0 \tan \beta l}, & n = m \end{cases} \tag{3.2.3}$$

where m and n are the entrance and exit branches of the transmission line, β is the phase constant and l is the line length. The term βl can also be written as $\beta l = \theta = 2\pi f T_d$, where T_d is the propagation delay (s) of the transmission line and f is the frequency of operation (Hz). The relationship of branch voltage V_z over branch element Y_z producing branch current I_z is described by:

$$\mathbf{I}_z = \mathbf{Y}_z \mathbf{V}_z \tag{3.2.4}$$

Voltages in a lumped element network that are defined with reference to a ground node are called node voltages $\mathbf{V}_n$. From Chua and Lin [44], the relationship between node voltages and branch voltages is given by:

$$\mathbf{V}_z = \mathbf{A}^t \mathbf{V}_n \tag{3.2.5}$$

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and the relationship between the mesh currents ($\mathbf{I}_n$) and branch currents follow as:

$$\mathbf{I}_n = \mathbf{A}\mathbf{I}_z \tag{3.2.6}$$

By substituting Eqs. 3.2.5 and 3.2.6 into Eq. 3.2.4, a relationship between node voltages, mesh currents and the incidence matrix of a network is found [44]:

$$\begin{aligned} \mathbf{A}\mathbf{I}_n &= \mathbf{A}\mathbf{Y}_z\mathbf{A}^t\mathbf{V}_n \\ \mathbf{I}_n &= \mathbf{A}\mathbf{Y}_z\mathbf{A}^t\mathbf{V}_n \end{aligned} \tag{3.2.7}$$

From Eq. 3.2.7, the node admittance matrix is defined as:

$$\mathbf{Y}_n \triangleq \mathbf{A}\mathbf{Y}_z\mathbf{A}^t \tag{3.2.8}$$

By applying a current source vector $\mathbf{I}_n$, the resulting node voltages are calculated by solving a set of independent linear equations.

This section introduced the incidence matrix and its application to node voltage analysis. Writing circuit simulation code is greatly simplified when the incidence matrix is used to solve nodal equations. The nodal solution can now be used in the calculation of a network's output sensitivities.

3.3 Sensitivity analysis by the adjoint method

Classical sensitivity analysis uses Tellegen's theorem aided by an ajoint *network*. The adjoint network is a duplicate (not for controlled sources) of the original network, but with a different excitation. Both circuits have to be solved to find the original network's sensitivities.

The adjoint *method* follows a different, but much more intuitive, approach. The matrix adjoint method is described in Section 3.3.1.

For sensitivity analysis to be a useful tool, the calculated results have to be interpreted meaningfully. Section 3.3.2 discusses how a network's output sensitivities are utilised.

Section 3.3.3 continues the series quarter-wave attenuator example from Fig. 3.1a by calculating its sensitivities. Furthermore, insights into the use of sensitivity results are given. Section 3.3.4 examines the different tolerance errors that occur in a microstrip circuit. Finally, a single error measure is defined in Section 3.3.5, where variation in output magnitude and phase due to element tolerances is shown.

3.3.1 Deriving the equations

Normalised sensitivity is defined as [4]:

$$S_{g_i}^{X_{out}} = \frac{\partial X_{out}}{\partial g_i}\frac{g_i}{X_{out}} \tag{3.3.1}$$

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where X_{out} is a linear combination of mesh currents and nodal voltages, and g_i is the value of the i'th component in the circuit. X_{out} is defined as:

$$X_{out} = \mathbf{c}^t \mathbf{V}_n + \mathbf{b}^t \mathbf{I}_n \tag{3.3.2}$$

where $\mathbf{c}$ and $\mathbf{b}$ are column vectors that select the relevant port current or node voltage as output. For $\mathbf{c}$, the voltage is chosen with a 1 or 0. Take $\mathbf{b}$ as 0. We are solving the node voltages and will only need $\mathbf{c}$ to select an output voltage.

To illustrate the output selection vector, consider the series quarter-wave attenuator in Fig. 3.1a. For a given f_0 and R_d, its nodal voltages are represented by:

$$\mathbf{V}_n = [V_1 \;\; V_2 \;\; V_3]^t \tag{3.3.3}$$

Clearly the desired output voltage is at node 3, hence the output selection vector is $\mathbf{c}^t = [0 \;\; 0 \;\; 1]$.

Once X_{out} is selected, its output sensitivities are determined by calculating its partial derivative with respect to each component g_i in the network: $\frac{\partial X_{out}}{\partial g_i}$. By taking the partial derivative, the relative changes in X_{out} for absolute changes in g_i is solved.

In further derivations, assume that node voltages and mesh currents are used. To find X_{out}, the nodal voltages of the network have to be solved first:

$$\mathbf{I} = \mathbf{Y}\mathbf{V} \tag{3.3.4}$$

Taking the derivative of Eq. 3.3.4 with respect to the components g_i in the node admittance matrix $\mathbf{Y}$, and applying the chain rule [45]:

$$\begin{aligned} \frac{d\mathbf{I}}{dg_i} &= \frac{\partial \mathbf{Y}}{\partial g_i}\mathbf{V} + \mathbf{Y}\frac{\partial \mathbf{V}}{\partial g_i} \\ 0 &= \frac{\partial \mathbf{Y}}{\partial g_i}\mathbf{V} + \mathbf{Y}\frac{\partial \mathbf{V}}{\partial g_i} \end{aligned} \tag{3.3.5}$$

Since the source vector $\mathbf{I}$ does not contain any components of $\mathbf{g}$, its derivative is zero.

Making the derivative of the node voltages the subject of the equation:

$$\begin{aligned} \mathbf{Y}\frac{\partial \mathbf{V}}{\partial g_i} &= -\frac{\partial \mathbf{Y}}{\partial g_i}\mathbf{V} \\ \frac{\partial \mathbf{V}}{\partial g_i} &= -\mathbf{Y}^{-1}\frac{\partial \mathbf{Y}}{\partial g_i}\mathbf{V} \end{aligned} \tag{3.3.6}$$

and premultiplying Eq. 3.3.6 by the output selection vector $\mathbf{c}^t$:

$$\begin{aligned} \mathbf{c}^t\frac{\partial \mathbf{V}}{\partial g_i} &= -\mathbf{c}^t\mathbf{Y}^{-1}\frac{\partial \mathbf{Y}}{\partial g_i}\mathbf{V} \\ \frac{\partial X_{out}}{\partial g_i} &= -\mathbf{c}^t\mathbf{Y}^{-1}\frac{\partial \mathbf{Y}}{\partial g_i}\mathbf{V} \end{aligned} \tag{3.3.7}$$

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Substituting $\mathbf{c}^t\mathbf{V}$ with X_{out}, the partial derivatives of X_{out} with respect to network components $\mathbf{g}$ is found.

Eq. 3.3.7 requires that the inverse of the admittance matrix $\mathbf{Y}$ be calculated. For small circuits this is computationally not a problem. However, for larger circuits calculating the inverse of a matrix becomes cumbersome. To avoid the calculation of the matrix inverse, the adjoint method is used by defining an adjoint vector $\mathbf{a}^t$ as in Eq. 3.3.8. Two properties of transpose matrices are used to solve for $\mathbf{a}^t$, namely $(\mathbf{A}^t)^t = \mathbf{A}$, and $(\mathbf{AB})^t = \mathbf{B}^t\mathbf{A}^t$ [46].

$$\begin{aligned} \mathbf{a}^t &= \mathbf{c}^t\mathbf{Y}^{-1} \\ \mathbf{a} &= (\mathbf{Y}^{-1})^t\mathbf{c} \\ \mathbf{Y}^t\mathbf{a} &= \mathbf{c} \end{aligned} \tag{3.3.8}$$

The adjoint vector $\mathbf{a}$ is found by solving the set of linear equations in Eq. 3.3.8. From Eq. 3.3.7, the derivative is:

$$\frac{\partial X_{out}}{\partial g_i} = -\mathbf{a}^t\frac{\partial \mathbf{Y}}{\partial g_i}\mathbf{V} \tag{3.3.9}$$

The sensitivity of the circuit is given by:

$$S_{g_i}^{X_{out}} = -\mathbf{a}^t\frac{\partial \mathbf{Y}}{\partial g_i}\mathbf{V}\frac{g_i}{X_{out}} \tag{3.3.10}$$

Eq. 3.3.10 gives multiple sensitivities for small relative variations in $\mathbf{g}$.

3.3.2 Magnitude and phase sensitivities

Eq. 3.3.10 results in multiple complex valued output sensitivities. For every variation in component value there is a corresponding variation in the output magnitude and transmission phase. However, the complex values calculated in Eq. 3.3.10 are not directly related to the output magnitude and phase. Consider again the sensitivity definition, which can also be written as:

$$\begin{aligned} S_{g_i}^{X_{out}} &= \frac{g_i\partial X_{out}}{X_{out}\partial g_i} \\ &= \frac{\partial \ln(X_{out})}{\partial \ln(g_i)} \end{aligned} \tag{3.3.11}$$

For steady state conditions, the output variable $X_{out}(j\omega)$ is written in polar form $X_{out}(j\omega) = |X_{out}|e^{(j\angle(X_{out}))}$ [4]. Taking the natural logarithm of the output variable:

$$\ln(X_{out}(j\omega)) = \ln|X_{out}(j\omega)| + j\angle(X_{out}(j\omega)) \tag{3.3.12}$$

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and substituting it into Eq. 3.3.11 gives:

$$\begin{aligned}\frac{g_i \partial X_{out}}{X_{out} \partial g_i} &= \frac{g_i \partial \ln X_{out}}{\partial g_i} \\ &= \frac{g_i \partial (\ln |X_{out}| + j \angle (X_{out}))}{\partial g_i} \\ &= \frac{g_i \partial |X_{out}|}{|X_{out}| \partial g_i} + j \frac{g_i \partial \angle (X_{out})}{\partial g_i}\end{aligned} \tag{3.3.13}$$

Eq. 3.3.13 shows the ith magnitude and phase sensitivity of X_{out}.

The real component of Eq. 3.3.13 gives the relative change in X_{out}'s amplitude due to relative change in component value [4]:

$$\mathrm{Re}\left(S_{g_i}^{X_{out}}\right) = \frac{g_i \partial |X_{out}|}{|X_{out}| \partial g_i} \tag{3.3.14}$$

and the imaginary component gives the absolute change in phase of X_{out} for a relative change in component value [4]:

$$\mathrm{Im}\left(S_{g_i}^{X_{out}}\right) = \frac{g_i \partial \angle (X_{out})}{\partial g_i} \tag{3.3.15}$$

in radians.

3.3.3 Example: Series quarter-wave attenuator

Consider again Fig. 3.1a where the circuit diagram of an ideal series quarter-wave attenuator is shown. To apply sensitivity analysis to this circuit, use nodal voltage analysis to obtain $\mathbf{V}$ and X_{out}. The branch admittance matrix is:

$$\mathbf{Y}_z = \begin{bmatrix} \frac{1}{R_{in}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{R_{50}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{R_{d1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{jZ_0 \tan \beta l} & \frac{j}{Z_0 \sin \beta l} & 0 & 0 \\ 0 & 0 & 0 & \frac{j}{Z_0 \sin \beta l} & \frac{1}{jZ_0 \tan \beta l} & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & \frac{1}{R_{d2}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{out}} \end{bmatrix}$$

T_1 in Fig. 3.1a is a quarter-wavelength line at the center frequency, $\beta l = 90^o$, $\sin \beta l = 1$ and $\tan \beta l$ becomes infinitely large. The nodal voltages are found by applying a source current $I_{in} = 0.04\ A$ in a 50 Ω system at node 1, translating to a 2 V open circuit source voltage. Solving the linear set of equations:

$$\mathbf{I} = \mathbf{A}\mathbf{Y}_z\mathbf{A}^t\mathbf{V} \tag{3.3.16}$$

The output is selected with:

$$X_{out} = [0\ \ 0\ \ 1]\mathbf{V} \tag{3.3.17}$$

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To solve the sensitivities, the derivative of $\mathbf{Y}_z$ is found in terms of $\mathbf{g} = [R_{in}, R_{50}, R_{d1}, R_{d2}, R_{out}, Z_0, T_d]$ respectively. The adjoint vector $\mathbf{a}^t$ is calculated as in Eq. 3.3.8.

The magnitude and phase sensitivities of each component to the output voltage are given in Figs. 3.2, 3.3 and 3.4 for $R_{d1} = R_{d2} = 1\ \Omega$, $Z_0 = 50\ \Omega$ and $T_d = 192.3\ ps$. The PIN diode resistor values were chosen arbitrarily.

There are seven output magnitude and seven output phase sensitivities.

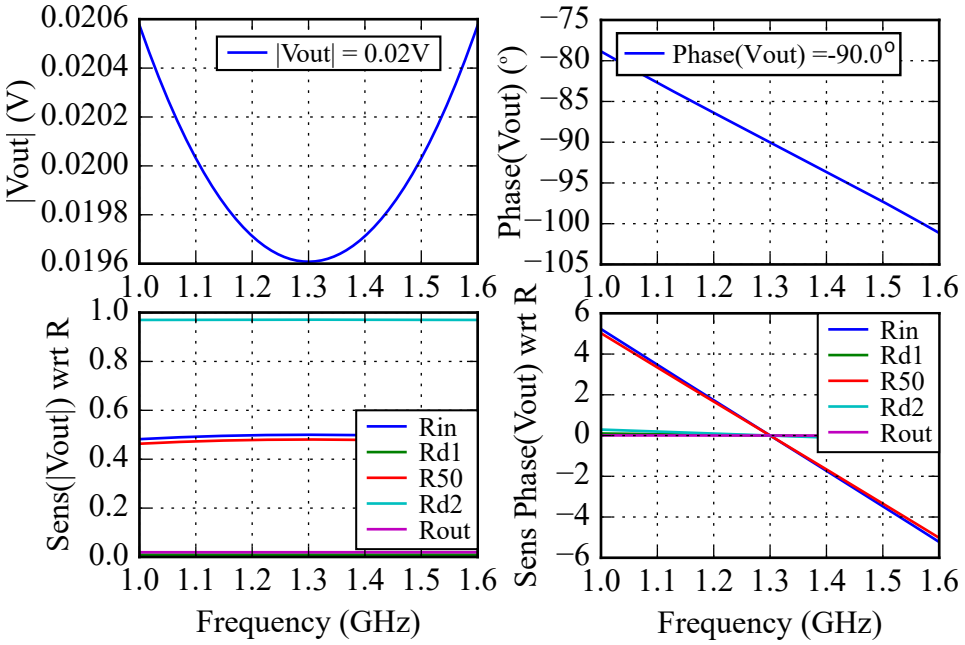

Figure 3.2: Output magnitude and phase sensitivities of V_{out} in terms of all the resistances in the circuit. The sensitivity of the output phase with respect to resistance variations was converted to degrees (^{o}).

Using Eqs. 3.3.14 and 3.3.15, the magnitude and phase sensitivities can be interpreted.

For a 10 % variation in R_{d2} at 1.3 GHz, the relative change in output magnitude is:

$$\Delta|X_{out}| \approx \frac{\mathrm{Re}\left(S_{R_{d2}}^{X_{out}}\right)|X_{out}|\Delta R_{d2}}{R_{d2}} \tag{3.3.18}$$

$$\approx 1 \text{ x } 0.01961 \text{ x } 0.1 = 0.001961\ V$$

For this example, the output magnitude (19.6 mV) increases by about 1.96 mV for a 10 % variation in R_{d2}. At 1.3 GHz, the resistors do not affect the output phase.

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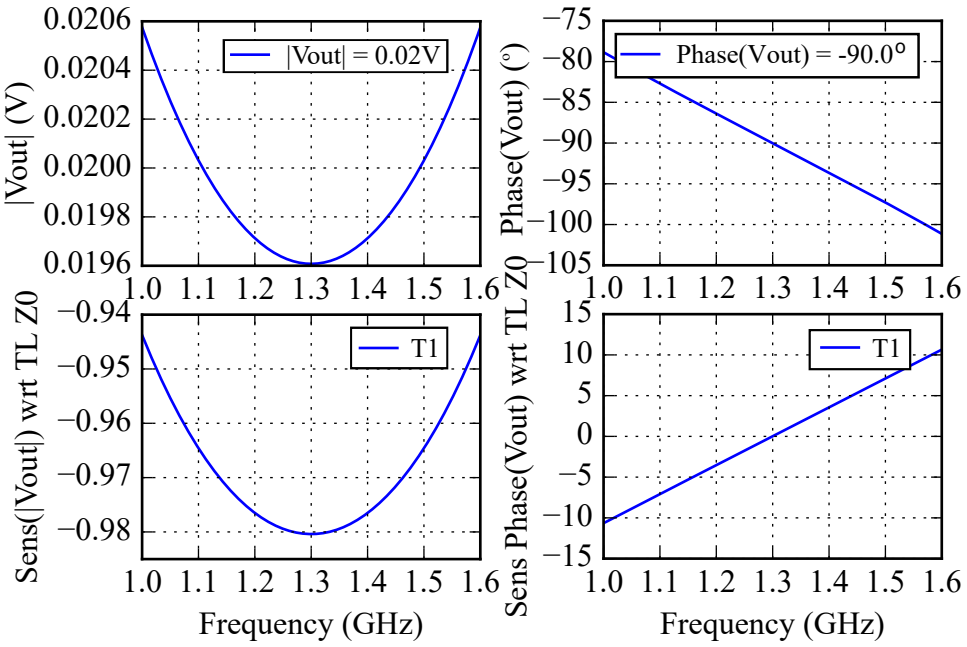

Figure 3.3: Output magnitude and phase errors of V_{out} in terms of the transmission line's Z_0. The sensitivity of the output phase with respect to Z_0 variations was converted to degrees (^{o}).

For an arbitrary 10 % variation in the propagation delay, the absolute change in output phase is:

$$\Delta\angle X_{out} \approx \frac{\mathrm{Im}\left(S_{T_1}^{X_{out}}\right)\Delta T_1}{T_1} \approx -47 \text{ x } 0.1 = -4.7\ ^o \tag{3.3.19}$$

A 10 % variation in T_d gives an output phase change of $-4.7\ ^o$. However, changing T_1's T_d by 10 % can also affect the output magnitude.

When a single component is changed for a particular output variation, ensure that the component does not have any further critical dependencies in magnitude or phase. The total effect that small component value variations have on the output is not obvious from the multiple output sensitivities. Clearly, a single error measure would ease the interpretation of multiple circuit sensitivities.

3.3.4 Summing sensitivities

For a random selection of elements, each with a variation $\frac{\Delta g_i}{g_i}$ around the nominal value of g_i, the expected RMS magnitude error of X_{out} for each component is estimated using:

$$\frac{\Delta|X_{out}|}{|X_{out}|} \approx \mathrm{Re}\left(S_{g_i}^{X_{out}}\right)\frac{\Delta g_i}{g_i} \tag{3.3.20}$$

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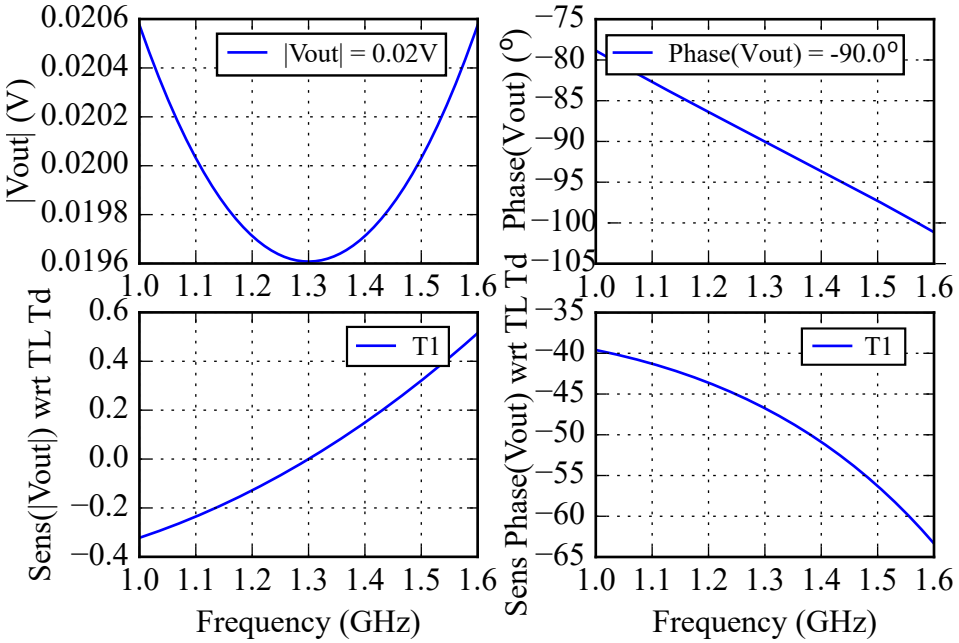

Figure 3.4: Output magnitude and phase errors of V_{out} in terms of the transmission line's T_d. The sensitivity of the output phase with respect to T_d variations was converted to degrees (^{o}).

and the expected RMS phase error of X_{out} for each component:

$$\Delta\angle(X_{out}) \approx \mathrm{Im}\left(S_{g_i}^{X_{out}}\right)\frac{\Delta g_i}{g_i} \ \ (radians) \tag{3.3.21}$$

The expected RMS magnitude and phase error in the above equations give multiple output variations in both magnitude and phase.

The combined effect of component tolerances on the output can not be determined by looking at the individual variations.

For further analysis, an output variable $\varphi(j\omega)$ is defined. The definition of a single output error measure through the addition of the squared variations of lumped and distributed elements is given.

3.3.4.1 Lumped elements

Assume that the resistances, inductances and capacitances in the network are uncorrelated from one another. The expected RMS magnitude error of the output X_{out} is estimated by adding the squares of uncorrelated sensitivities directly:

$$\frac{\Delta|\varphi|}{|X_{out}|} = \sqrt{\sum_i \left(\mathrm{Re}\left(S_{g_i}^{X_{out}}\right)\frac{\Delta g_i}{g_i}\right)^2} \tag{3.3.22}$$

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The expected RMS phase error of X_{out} due to lumped element tolerances is estimated from:

$$\Delta\angle\varphi = \sqrt{\sum_i \left(\mathrm{Im}\left(S_{g_i}^{X_{out}}\right)\frac{\Delta g_i}{g_i}\right)^2} \tag{3.3.23}$$

The lumped elements are uncorrelated since the variation between element values is not related. Correlated elements refer to components that have dependent variations.

3.3.4.2 Distributed elements

Transmission lines are modelled using two port Y parameters as discussed in Section 3.2.2. For networks that are implemented on microstrip, there exist tolerances in the substrate's height and relative dielectric constant [47], [48]. Some of the variations that occur in microstrip transmission lines due to tolerances are correlated.

Calculating Z_0's output sensitivity to microstrip dimensional tolerances is well documented [22], [49] and [50]. The characteristic impedance (Z_0) and propagation delay (T_d) of a microstrip transmission line both depend on the relative dielectric constant (ϵ_r) of the material as shown in Eqs. 3.3.24 to 3.3.27. The impedance equation for microstrip lines, where the ratio of the width of the microstrip line W to the dielectric height $h > 1$, is [51]:

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_e}[\frac{W}{h} + 1.393 + 0.667\ln(\frac{W}{h} + 1.444)]} \tag{3.3.24}$$

where ϵ_e is the effective dielectric constant. The effective dielectric constant is a function of the relative dielectric constant ϵ_r [51]:

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\frac{1}{\sqrt{1 + \frac{12h}{W}}} \tag{3.3.25}$$

Eq. 3.3.24 is also dependent on the substrate height (h) and trace width (W). If the circuit is manufactured with a large trace width, the error due to trace width tolerance is negligible. Substrate height h tolerance is included in the analysis.

Propagation delay is calculated using [51]:

$$T_d = \frac{\beta l}{2\pi f} \tag{3.3.26}$$

where βl is the phase delay in radians and f is the frequency in Hz. The propagation constant β of a microstrip line is expressed as [51]:

$$\beta = k_0\sqrt{\epsilon_e} \tag{3.3.27}$$

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The propagation constant and characteristic impedance can now be expressed as a function of their variables:

$$\begin{aligned} T_d &= f(\epsilon_e) \\ Z_0 &= f(\epsilon_e, h) \\ \epsilon_e &= f(\epsilon_r, h) \end{aligned} \tag{3.3.28}$$

Z_0 is a function of both ϵ_e and h. By using the chain rule, the partial derivative of Z_0 is found in terms of ϵ_e and h:

$$\frac{dZ_0}{d\epsilon_e} = \frac{\partial Z_0}{\partial \epsilon_e} + \frac{\partial Z_0}{\partial h}\frac{dh}{d\epsilon_e} \tag{3.3.29}$$

and

$$\frac{dZ_0}{dh} = \frac{\partial Z_0}{\partial h} + \frac{\partial Z_0}{\partial \epsilon_e}\frac{d\epsilon_e}{dh} \tag{3.3.30}$$

In Eq. 3.3.29 the substrate height is not dependent on the dielectric constant, therefore the second term of the equation is zero. The effective dielectric constant is also dependent on two variables, its partial derivatives in terms of ϵ_r and h are:

$$\frac{d\epsilon_e}{d\epsilon_r} = \frac{\partial \epsilon_e}{\partial \epsilon_r}\frac{d\epsilon_r}{d\epsilon_r} + \frac{\partial \epsilon_e}{\partial h}\frac{dh}{d\epsilon_r} \tag{3.3.31}$$

$$\frac{d\epsilon_e}{dh} = \frac{\partial \epsilon_e}{\partial h}\frac{dh}{dh} + \frac{\partial \epsilon_e}{\partial \epsilon_r}\frac{d\epsilon_r}{dh} \tag{3.3.32}$$

Both the terms $\frac{dh}{d\epsilon_r}$ and $\frac{d\epsilon_r}{dh}$ are zero, and the above equations become:

$$\frac{d\epsilon_e}{d\epsilon_r} = \frac{\partial \epsilon_e}{\partial \epsilon_r} \tag{3.3.33}$$

$$\frac{d\epsilon_e}{dh} = \frac{\partial \epsilon_e}{\partial h} \tag{3.3.34}$$

If Z_0 and T_d sensitivities are represented by $S_{Z_0}^{X_{out}}$ and $S_{T_d}^{X_{out}}$, using the sensitivity property:

$$S_z^y = S_x^y S_z^x \tag{3.3.35}$$

the sensitivity of the output to variations in the relative dielectric constant ϵ_r is found using:

$$S_{\epsilon_r}^{X_{out}} = S_{Z_0}^{X_{out}} S_{\epsilon_e}^{Z_0} S_{\epsilon_r}^{\epsilon_e} + S_{T_d}^{X_{out}} S_{\epsilon_e}^{T_d} S_{\epsilon_r}^{\epsilon_e} \tag{3.3.36}$$

The output sensitivity to substrate height tolerance is:

$$S_h^{X_{out}} = S_{Z_0}^{X_{out}} S_h^{Z_0} \tag{3.3.37}$$

where $S_h^{Z_0}$ is calculated from Eq. 3.3.30. This analysis can be repeated for temperature dependence.

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The relative dielectric constant's tolerance is found on the substrate's datasheet. For *RO4003C*, the typical ϵ_r tolerance is 1.5 % and substrate height tolerance is typically 7 %. The substrate height tolerance maintains a similar value for changing substrate thickness larger than 8 *mil* [48]. The substrate height tolerance is significantly larger for a substrate height of 8 *mil* (12.5 %).

The sensitivities in terms of ϵ_r and h are uncorrelated, they are also uncorrelated with the lumped elements. The squares of the magnitude and phase sensitivities in terms of ϵ_r and h are added directly with the lumped magnitude and phase sensitivities. From these results, a single error measure is defined.

3.3.5 Magnitude and phase error measure

A single error measure in terms of magnitude and phase sensitivities is found by taking the square root of the sum of the squared magnitude and phase errors (RSS). Correlated sensitivities are summed before being added to the RSS measure. The RSS magnitude error is estimated as:

$$\begin{aligned}\frac{|\varphi|_{RSS}}{|X_{out}|} &= \sqrt{\sum_i \left(\mathrm{Re}\left(S_{g_i}^{X_{out}}\right)\frac{\Delta g_i}{g_i}\right)^2} \\ &= \Bigg\{\left(\sum_i \mathrm{Re}\left(S_{\epsilon_{ri}}^{X_{out}}\right)\frac{\Delta\epsilon_r}{\epsilon_r}\right)^2 + \sum_j \left(\mathrm{Re}\left(S_{R_j}^{X_{out}}\right)\frac{\Delta R}{R}\right)^2 \\ &\quad + \sum_k \left(\mathrm{Re}\left(S_{L_k}^{X_{out}}\right)\frac{\Delta L}{L}\right)^2 + \sum_l \left(\mathrm{Re}\left(S_{C_l}^{X_{out}}\right)\frac{\Delta C}{C}\right)^2 \\ &\quad + \left(\sum_m \mathrm{Re}\left(S_{h_m}^{X_{out}}\right)\frac{\Delta h}{h}\right)^2\Bigg\}^{\frac{1}{2}}\end{aligned} \tag{3.3.38}$$

and the RSS phase error is estimated as:

$$\begin{aligned}\angle\varphi_{RSS} &= \sqrt{\sum_i \left(\mathrm{Im}\left(S_{g_i}^{X_{out}}\right)\frac{\Delta g_i}{g_i}\right)^2} \\ &= \Bigg\{\left(\sum_i \mathrm{Im}\left(S_{\epsilon_{ri}}^{X_{out}}\right)\frac{\Delta\epsilon_r}{\epsilon_r}\right)^2 + \sum_j \left(\mathrm{Im}\left(S_{R_j}^{X_{out}}\right)\frac{\Delta R}{R}\right)^2 \\ &\quad + \sum_k \left(\mathrm{Im}\left(S_{L_k}^{X_{out}}\right)\frac{\Delta L}{L}\right)^2 + \sum_l \left(\mathrm{Im}\left(S_{C_l}^{X_{out}}\right)\frac{\Delta C}{C}\right)^2 \\ &\quad + \left(\sum_m \mathrm{Im}\left(S_{h_m}^{X_{out}}\right)\frac{\Delta h}{h}\right)^2\Bigg\}^{\frac{1}{2}}\end{aligned} \tag{3.3.39}$$

These error measures indicate the expected RMS error that will occur within a set of electrical networks due to component tolerances.

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Consider again the series quarter-wave attenuator example, its RSS magnitude and phase errors are shown in Fig. 3.5. Assume typical lumped element tolerances of 10 %, ϵ_r tolerance of 1.5 % and substrate height h tolerance of 7 %. The RSS phase error in Fig. 3.5 is the expected RMS phase error

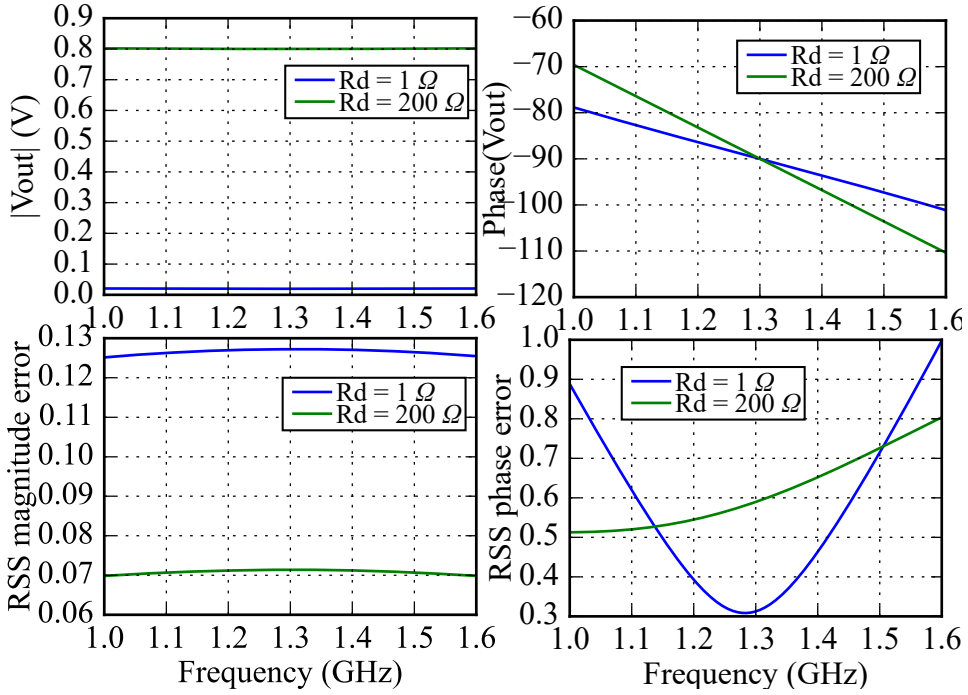

Figure 3.5: The normalised RSS magnitude and RSS phase errors of the series quarter-wave attenuator for $R_d = 1\ \Omega$ and $R_d = 200\ \Omega$. Phase(V_{out}) and the RSS phase error is given in degrees.

due to component tolerances. The series quarter-wave attenuator has a very low phase tracking error. However, the PIN diode model used in the simulation was purely resistive so the RSS phase error in Fig. 3.5 is because of the transmission line tolerances only.

3.4 Conclusion

Nodal voltage analysis using the incidence matrix was described for lumped and distributed elements. It was shown that automation of circuit analysis is greatly simplified when the incidence matrix is used.

Sensitivity analysis by the adjoint method in the frequency domain was defined. A method to derive the sensitivity of a linear circuit containing distributed elements as well as lumped elements was given. Finally, the interpretation of a linear network's sensitivity results was discussed.

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Existing sensitivity analysis was extended to include lumped and distributed elements. The output sensitivities of a network was derived using a mathematical approach instead of Tellegen's theorem and the adjoint circuit. A unified basis was created from which sensitivity analysis could be performed on a network containing both lumped and distributed elements.

Furthermore, an effective sensitivity error measure was defined from output sensitivity results. The newly defined sensitivity error measure is suitable to rank the phase tracking performance of multiple electronic networks.

A set of phase tracking EVAs is needed for a multi-channel receiver with strict phase tracking requirements. In Chapter 4, the RSS error measure is used to grade the phase tracking of several families of EVAs.

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Chapter 4

Optimal Phase Tracking Electronically Variable Attenuators

4.1 Introduction

Electronically variable attenuators (EVAs) provide STC for multi-channel DBF radar receivers. When good phase tracking between channels of a multi-channel receiver is required, EVAs also need to track in phase over their full control range.

EVAs are placed before the first low noise amplifier (LNA) in the receivers of a multi-channel DBF radar. Insertion loss added before the first LNA adds directly to a receiver's noise figure. The optimal set of phase tracking EVAs need minimal insertion loss to reduce its effect on the receiver's noise figure. Commercially available digital attenuators typically have insertion loss larger than 2 dB.

EVAs use PIN diodes as current controlled resistors. By controlling the biasing current applied to each PIN diode, the EVA's transmission coefficient is varied. At high frequencies PIN diodes have a complex impedance determined by bond wire inductance and junction capacitance. The PIN diode's small signal model was briefly discussed in Chapter 2.

PIN diode impedance tolerance together with distributed line tolerance causes phase tracking errors within a set of EVAs. PIN diode resistances typically have a variation of 10 % around its nominal value [5]. Manufactured transmission lines have dimensional tolerances [52].

In Chapter 3, an RSS error measure was derived using output sensitivity results. The RSS phase error measure gives the expected RMS phase error within a set of networks due to tolerances in the network. By calculating the RSS phase error of several matched EVAs, their phase tracking errors are ranked over control range. The RSS error measure method identifies an opti-

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mal phase tracking set of EVAs from the topologies that are analysed. Individual component sensitivity results are also used to improve current available designs.

Section 4.2 gives the RSS phase error of several EVAs, where matched EVAs are compared over control range in terms of their RSS phase tracking error. In Section 4.2, a set of cascade parallel quarter-wave attenuators (CPQA) is identified as having optimal phase tracking over its full control range. The CPQA is investigated further in terms of its transmission and reflection coefficients, power handling and biasing network in Section 4.3. A test set-up to measure the phase tracking of a set of CPQAs is given in Section 4.4. Finally, measurements confirming the CPQA's good phase tracking are discussed in Section 4.5.

An optimal phase tracking set of L-band EVAs is identified through an RSS phase error measure defined from output sensitivity results.

4.2 Sensitivity analysis of electronically variable attenuators

Chapter 2 describes typical matched attenuators that can readily be found [1]. Matched attenuators have a good input and output match over the control range. A good match helps to reduce phase tracking errors caused by signals that are re-reflected from external circuitry. An equation for each attenuator's output attenuation versus PIN diode resistance R_d was given in Chapter 2. The matched EVA topologies that will be discussed in this chapter are:

1. Series hybrid attenuator (similar results are obtained with parallel hybrid attenuator) [1].

2. Double hybrid attenuator [1].

3. Parallel quarter-wave attenuator [1].

4. Cascade parallel quarter-wave attenuator (CPQA) as proposed by Walker [32] and implemented in [33].
   This topology has not been documented extensively in the available literature.

5. Series quarter-wave attenuator [1].

6. Cascade series quarter-wave attenuator (CSQA).
   The CSQA has not been documented in available literature.

The two cascaded topologies have not been defined with equations that describe its transmission coefficient. By using node voltage analysis, an equation

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for the CPQA's transmission coefficient is derived in terms of R_d:

$$|S_{21}| = \frac{Z_0^2(R_d + Z_0)^2}{Z_0^4 + 4R_dZ_0^3 + 6R_d^2Z_0^2 + 4R_d^3Z_0 + 2R_d^4} \tag{4.2.1}$$

The CPQA's transmission coefficient is derived for a purely resistive PIN diode (R_d).

The CSQA has to be defined in terms of its attenuation versus R_d as well. Following the same process as for the CPQA, an equation for the CSQA's transmission coefficient is found:

$$|S_{21}| = \frac{R_d^2(R_d + Z_0)^2}{R_d^4 + 4Z_0R_d^3 + 6Z_0^2R_d^2 + 4Z_0^3R_d + 2Z_0^4} \tag{4.2.2}$$

Once again, a purely resistive model is used for the PIN diode resistance R_d.

The equivalent resistance (R_d) is calculated for each topology and summarised in Table 4.1 for attenuation $L = 1, 10, 25, 40\ dB$. These attenuation values are chosen arbitrarily to represent the attenuation range between 1 and 40 dB.

Table 4.1: Calculated resistance values for each matched attenuator over attenuation. In the listed equations, $Z_0 = 50\ \Omega$.

Equation	1 dB	10 dB	25 dB	40 dB
Series hybrid attenuator $20\log\left\{1 + \frac{2Z_0}{R_d}\right\}$	819 Ω	46 Ω	5.96 Ω	1 Ω
Double hybrid attenuator $20\log\left\{1 + \frac{Z_0}{2R_d}\right\}$	205 Ω	11.6 Ω	1.49 Ω	0.25 Ω
Parallel quarter-wave attenuator $20\log\left\{1 + \frac{R_d}{Z_0}\right\}$	6.1 Ω	108 Ω	839 Ω	4950 Ω
CPQA $20\log\left\{\frac{Z_0^2(R_d+Z_0)^2}{Z_0^4+4R_dZ_0^3+6R_d^2Z_0^2+4R_d^3Z_0+2R_d^4}\right\}$	3 Ω	37.5 Ω	136 Ω	349 Ω
Series quarter-wave attenuator $20\log\left\{1 + \frac{Z_0}{R_d}\right\}$	410 Ω	23 Ω	3 Ω	0.5Ω
CSQA $20\log\left\{\frac{R_d^2(R_d+Z_0)^2}{R_d^4+4Z_0R_d^3+6Z_0^2R_d^2+4Z_0^3R_d+2Z_0^4}\right\}$	840 Ω	66.5 Ω	18.4 Ω	7.2Ω

The equivalent impedance of some of the calculated resistances in Table 4.1 will be dominated by either the PIN diode's series inductance or junction capacitance.

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1. The double hybrid attenuator requires a 0.25 Ω PIN diode resistance to achieve 40 dB attenuation. When a realistic PIN diode model is used, the PIN diode's series inductance will completely swamp the minimum resistance value. For this reason, a PIN diode with a small series inductance is needed.

2. The parallel quarter-wave attenuator requires a 4950 Ω resistance to achieve 40 dB attenuation. This R_d value is unrealistic, the PIN diode's junction capacitance will make it impossible to achieve such a large equivalent impedance.

Some of the values in Table 4.1 are unrealistic due to PIN diode inductive and capacitive components. The ideal calculated resistor values are used in the following analysis to emphasise some of the topologies' limitations.

The RSS phase errors of the six matched attenuators listed in Table 4.1 are calculated over control range and frequency. By comparing the RSS phase error for each topology over attenuation range, it is possible to identify an optimal phase tracking set of EVAs. Realistic PIN diode impedances have to be taken into account when an optimal phase tracking EVA is identified. The output RSS phase errors are calculated for attenuation $L = 1, 10, 25, 40\ dB$.

For given component tolerances, the RSS phase error calculates the expected RMS phase error of a set of lumped and distributed networks. From Chapter 3, the RSS phase error is:

$$\Delta\varphi_{RSS} = \sqrt{\sum_i (S_{g_i}^{\angle Y_{out}} \frac{\Delta g_i}{g_i})^2} \tag{4.2.3}$$

The phase error measure is the sum of the square of the uncorrelated weighted individual output phase sensitivities. Correlated sensitivities are summed before being added to the squared lumped sensitivities.

To calculate a network's output sensitivity as defined in Chapter 3, typical PIN diode parameters are required. A PIN diode from *Infineon* (*BAR50-02*) is used with $L_s = 0.6\ nH$ and $C_j = 0.15\ pF$. This PIN diode is chosen because of its low series inductance and junction capacitance.

It was found in [5] that a PIN diode's resistance typically varies by 10 %. The PIN diode's capacitance and inductance also vary depending on the placement of the diode on the transmission line. Consequently, a tolerance of 10 % is chosen for all lumped elements. A dielectric constant tolerance of 1.5 % is used, and a substrate height tolerance of 7 %. The substrate related tolerances are typical values found on the Rogers RO4003 datasheet [47].

The RSS phase error of each topology will be discussed in terms of:

1. Good/Bad RSS phase error over control range.

2. *Additional*: Possible improvements to attenuator's response derived from output sensitivity results.

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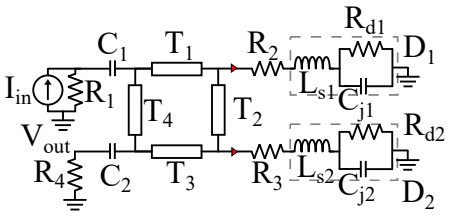
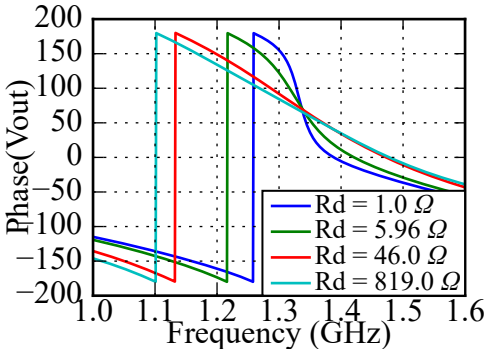
4.2.1 Series hybrid attenuator

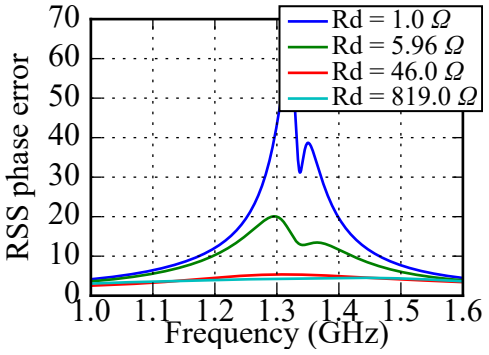
The circuit diagram of a series hybrid attenuator is given in Fig. 4.1a. Diodes D_1 and D_2 have been replaced by equivalent small signal models. It is typical to use a single current source for this topology (applied at T_2). The PIN diodes' resistance tracking error is taken into account.



(a) Circuit diagram.



(b) Transmission phase.



(c) RSS phase error.

Figure 4.1: The series hybrid attenuator's circuit diagram, its transmission phase and RSS phase error for $L = 1\ dB, 10\ dB, 25\ dB, 40\ dB$. Phase($V_{out}$) and the RSS phase error is given in degrees.

The series hybrid attenuator's transmission phase and RSS phase error are shown in Figs. 4.1b and 4.1c.

The RSS phase error is large over a range of PIN diode resistances. When R_d is small, the standard deviation of the error with respect to the nominal phase of a single series hybrid attenuator can deviate by more than 40 ^{o} at the center frequency. This means that the standard deviation of the difference between any two EVAs in a set of such EVAs is $\sqrt{2}40 \approx 56\ degrees$. Such a large phase discrepancy between attenuators in a multi-channel receiver will result in a significant DoA estimation error.

4.2.2 Double hybrid attenuator

Fig. 4.2a shows the small signal circuit diagram of a double hybrid attenuator. PIN diodes D_1 and D_2 have been replaced by their equivalent small signal models. A biasing current is applied to transmission line T_2, dividing the

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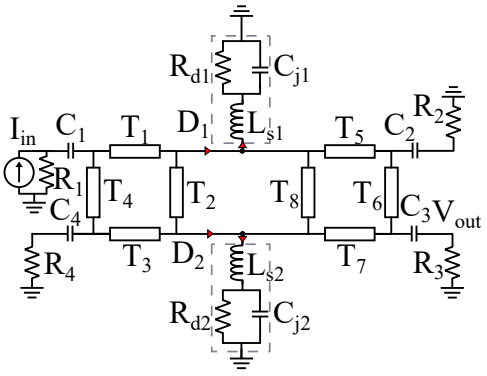
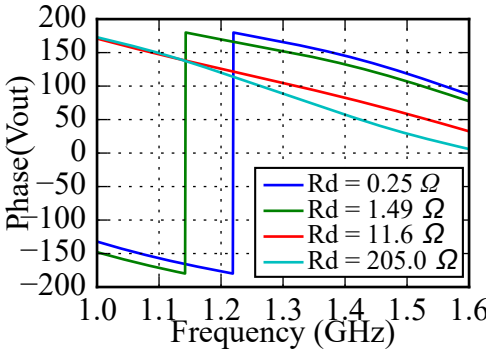
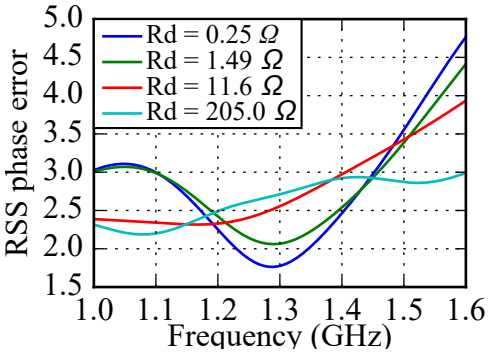
current between the two diodes. For the calculation of the double hybrid attenuator's RSS phase error, PIN diode resistance tracking error is taken into account.



(a) Circuit diagram.



(b) Transmission phase.



(c) RSS phase error.

Figure 4.2: The double hybrid attenuator's circuit diagram, transmission phase and RSS phase error for attenuation $L = 1\ dB, 10\ dB, 25\ dB, 40\ dB$. Phase($V_{out}$) and the RSS phase error is given in degrees.

The double hybrid attenuator's transmission phase over attenuation is shown in Fig. 4.2b, while its RSS phase error results are given in Fig. 4.2c.

The double hybrid attenuator's RSS phase error is much smaller over attenuation than that of the series hybrid attenuator. Within a set of double hybrid attenuators, the expected RMS phase error between attenuators will not be larger than $3\ ^o$ at the center frequency over the full control range. However, it is important to note that due to the presence of the series inductances L_{s1} and L_{s2}, the equivalent impedance of the PIN diodes when $R_d = 0.25\ \Omega$ does not result in 40 dB attenuation.

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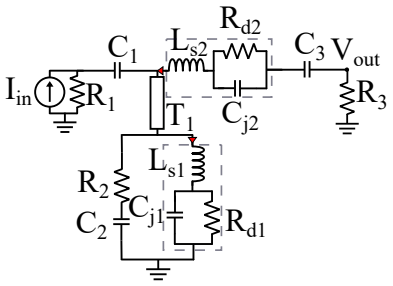
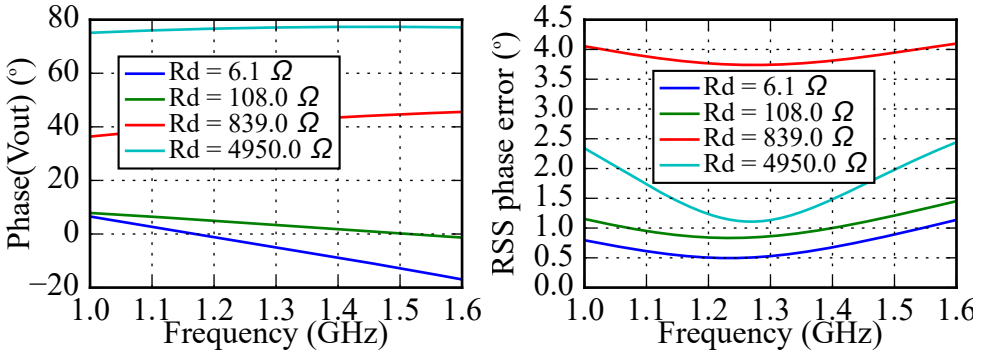
4.2.3 Parallel quarter-wave attenuator

A circuit diagram of the parallel quarter-wave attenuator is given in Fig. 4.3a. Diodes D_1 and D_2 have been replaced by their equivalent small signal models. For a parallel quarter-wave attenuator, an equal biasing current is applied to both PIN diodes. The PIN diodes' resistance tracking error is taken into account.



(a) Circuit diagram.



(b) Transmission phase.

(c) RSS phase error.

Figure 4.3: Parallel quarter-wave attenuator's circuit diagram, transmission phase and RSS phase error for $L = 1\ dB, 10\ dB, 25\ dB, 40\ dB$. Phase($V_{out}$) and the RSS phase error is given in degrees.

The transmission phase and RSS phase error of the parallel quarter-wave attenuator is shown in Figs. 4.3b and 4.3c.

The RSS phase error is small for small values of R_d . However, as R_d increases, so does the expected RMS phase error that can occur within a set of attenuators. Once R_d becomes comparable to the impedance of C_j, the RSS phase error decreases again. When C_j dominates the equivalent impedance, the attenuation of the parallel quarter-wave attenuator has reached its maximum achievable value.

The parallel quarter-wave attenuator is not matched at its output port and is not a good candidate for use in a receiver.

From Table 4.1, $R_d = 4950\ \Omega$ is an unrealistic value for a PIN diode since the true impedance is dominated by the parallel junction capacitance.

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Output sensitivity results are used to improve a parallel quarter-wave attenuator to obtain a better RSS phase error over its full control range.

4.2.3.1 Proposed improvement

An improvement to the parallel quarter-wave attenuator's output RSS phase error is found by considering the individual capacitances' output phase sensitivities in Fig. 4.4. Diode D_2's junction capacitance is the dominant contributor to the attenuator's increasing output phase error. Simultaneously, C_{j2} has almost no effect on the input phase sensitivity.

By cascading the parallel quarter-wave attenuator in a back-to-back configuration, the effect of PIN diode D_2's junction capacitance on the output phase error is reduced significantly. Furthermore, the cascaded configuration has the advantage of being matched at both its input and output port over control range. This cascaded parallel quarter-wave attenuator is discussed in

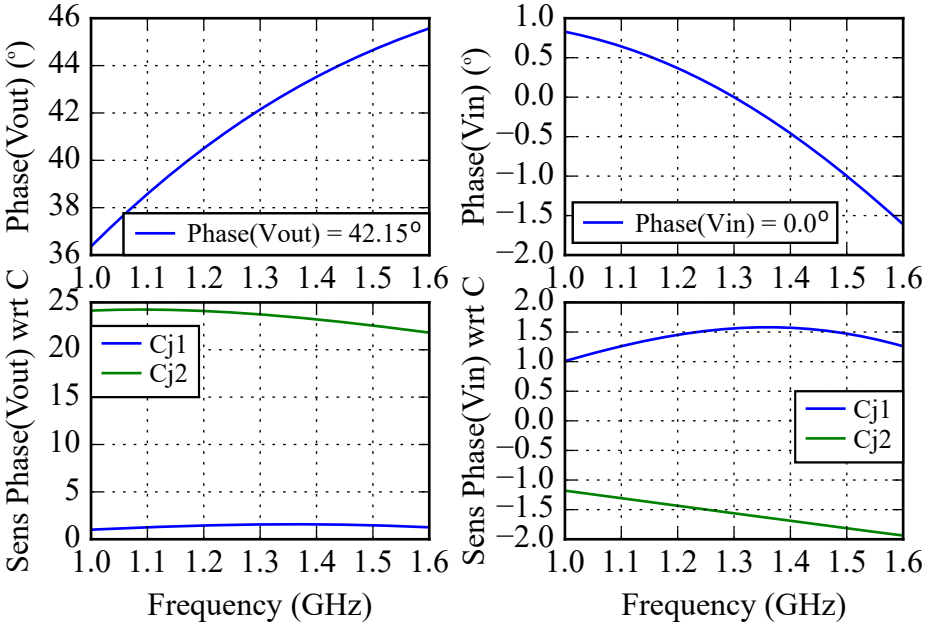

Figure 4.4: Input and output sensitivity of parallel quarter-wave attenuator with respect to diode junction capacitances at $R_d = 839\ \Omega$. The phase sensitivities are displayed in degrees.

the next section.

4.2.4 Cascade parallel quarter-wave attenuator

The CPQA's circuit diagram is shown in Fig. 4.5a. Diodes D_1, D_2, D_3 and D_4 have been replaced by their equivalent small signal models. Assume all

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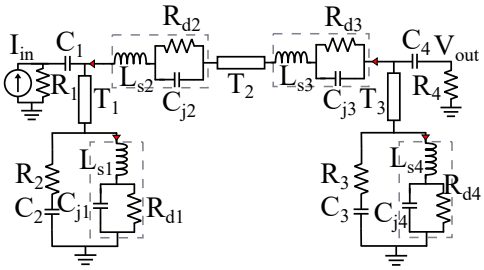
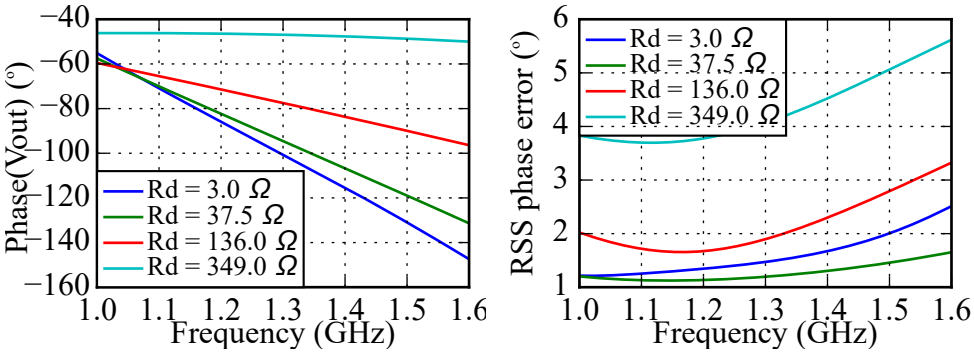
four PIN diodes are biased by a shared current. The PIN diodes' resistance tracking error is taken into account.



(a) Circuit diagram.



(b) Transmission phase.

(c) RSS phase error.

Figure 4.5: CPQA's circuit diagram, transmission phase and RSS phase error for attenuation $L = 1\ dB, 10\ dB, 25\ dB, 40\ dB$. Phase($V_{out}$) and the RSS phase error is given in degrees.

The transmission phase and RSS phase error of the CPQA are given in Figs. 4.5b and 4.5c.

The CPQA's RSS phase error is much lower over realistic control range than that of the series and double hybrid attenuators. Furthermore, the CPQA's RSS phase error remains similar over frequency. The only exception is when the CPQA provides 40 dB attenuation; the CPQA's RSS phase error is slightly higher than the double hybrid attenuator's RSS phase error. However, unlike the double hybrid attenuator in Fig. 4.2a, the CPQA can achieve 40 dB attenuation.

The double hybrid attenuator requires a PIN diode resistance of $R_d = 0.25\ \Omega$ to achieve 40 dB attenuation. When series inductance is taken into account, the double hybrid attenuator can not reach this low equivalent impedance and as a result can not be used over such a wide range of attenuation. The CPQA has a more realistic PIN diode resistance requirement ($3 - 349\ \Omega$) over the $1 - 40\ dB$ dynamic range.

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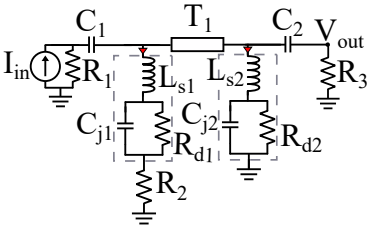
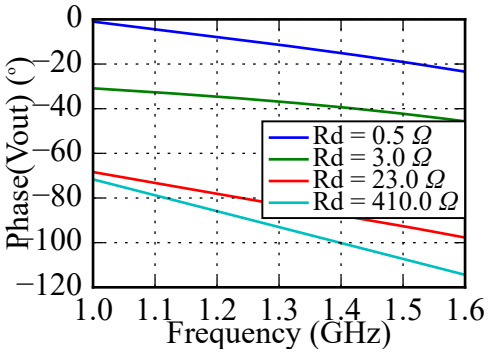
4.2.5 Series quarter-wave attenuator

The series quarter-wave attenuator's circuit diagram is shown in Fig. 4.6a. Diodes D_1 and D_2 have been replaced by their equivalent small signal model. Current is applied at R_{d2} and terminates to ground at R_2. The PIN diodes' resistance tracking error is taken into account.

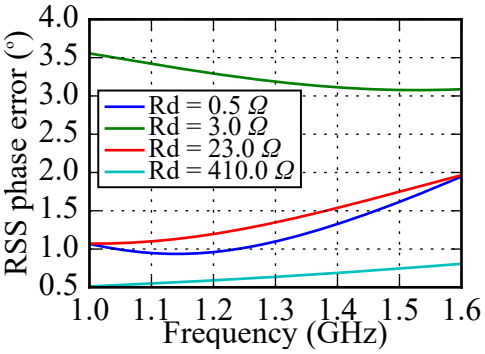
Figs. 4.6b and 4.6c give the series quarter-wave attenuator's transmission phase and RSS phase error.



(a) Circuit diagram.



(b) Transmission phase.



(c) RSS phase error.

Figure 4.6: Series quarter-wave attenuator's circuit diagram, transmission phase and RSS phase error for $L = 1\ dB, 10\ dB, 25\ dB, 40\ dB$. Phase($V_{out}$) and the RSS phase error is given in degrees.

The RSS phase error of the series quarter-wave attenuator increases significantly when $R_d = 3\,\Omega$. However, once R_d becomes smaller than L_s's equivalent impedance the RSS phase error remains relatively low. The series quarter-wave attenuator's maximum attenuation is limited by the equivalent impedance of the PIN diode's series inductance L_{s2}.

A disadvantage of this topology is that its output is not matched over its full control range. The series quarter-wave attenuator does not achieve the full 40 dB attenuation range since its equivalent PIN diode impedance is limited by the diode's series inductance.

Output sensitivity results are used to create a new cascaded attenuator topology with an improved output RSS phase error.

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4.2.5.1 Proposed improvement

Consider the individual component sensitivities of the series quarter-wave attenuator when $R_d = 3\ \Omega$. Fig. 4.7 shows the output phase sensitivity for small variations in the series inductance. The input's phase sensitivity to small variations in inductance is also given.

The largest output phase sensitivity is found for variation in the series inductance L_{s2}, but the input voltage is relatively insensitive to variations in L_{s2}.

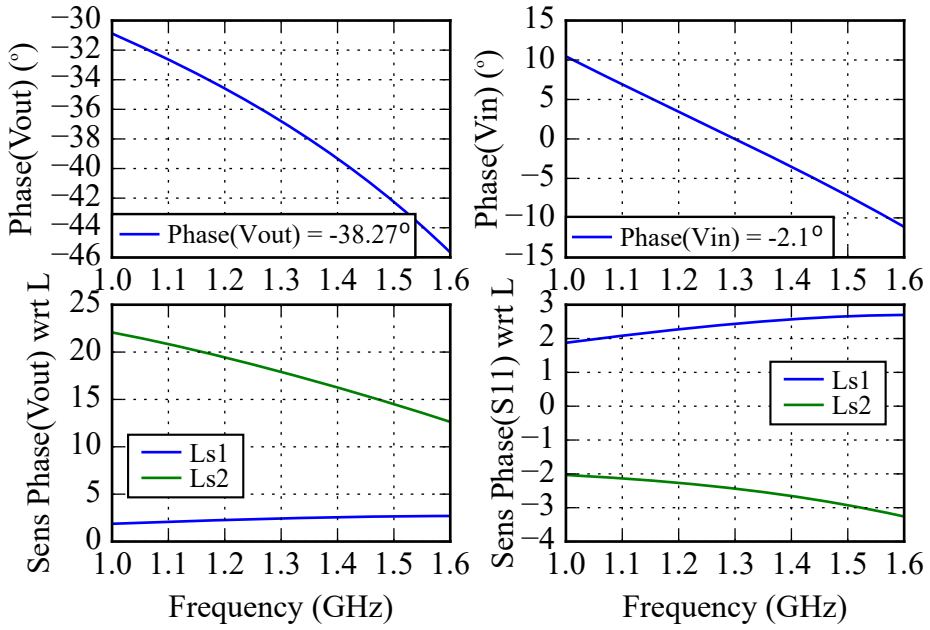

Figure 4.7: Input and output phase sensitivities due to the inductances in the series quarter-wave attenuator's PIN diodes when $R_d = 3\ \Omega$. The phase sensitivities are displayed in degrees.

A back-to-back cascaded topology removes the series quarter-wave attenuator's L_{s2} output sensitivity and simultaneously creates a new topology that is matched at its input and output port. The cascade series quarter-wave attenuator is discussed in the next section.

4.2.6 Cascade series quarter-wave attenuator

The new proposed cascade series quarter-wave attenuator (CSQA) circuit diagram is given in Fig. 4.8a. PIN diodes D_1, D_2, D_3 and D_4 are replaced with their equivalent small signal models. The PIN diodes' resistance tracking error is taken into account.

The CSQA transmission phase and RSS phase error over control range are shown in Figs. 4.8b and 4.8c.

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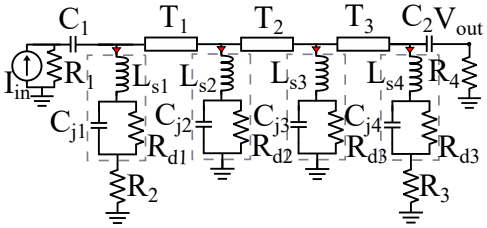
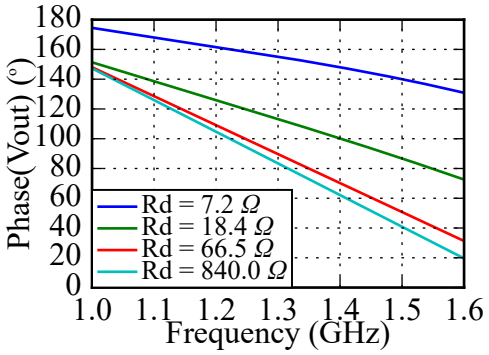
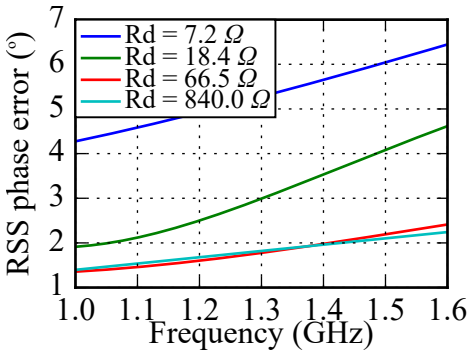


(a) Circuit diagram.



(b) Transmission phase.



(c) RSS phase error.

Figure 4.8: CSQA's circuit diagram, transmission phase and RSS phase error for $L = 1\ dB, 10\ dB, 25\ dB, 40\ dB$. Phase($V_{out}$) and the RSS phase error is given in degrees.

The RSS phase error is similar to the series quarter-wave attenuator case. However, the CSQA's RSS phase error is larger than the CPQA's.

The CSQA's smallest attenuation depends on the PIN diode's largest resistance. The PIN diode's impedance is limited by the junction capacitance when R_d and C_j have similar equivalent impedances.

4.2.7 Results summary

The RSS phase error results are summarised in Table 4.2. All the results are given at 1.3 GHz.

Table 4.2: Output RSS phase error (^{o}) results of EVA topologies at 1.3 GHz.

Attenuation	1 dB	10 dB	25 dB	40 dB
Series hybrid	4.26°	5.37°	20°	43.28°
Double hybrid	2.71°	2.56°	2.07°	1.776°
Parallel quarter-wave	0.53°	0.86°	3.74°	1.13°
CPQA	1.47°	1.20°	1.90°	4.07°
Series quarter-wave	0.67°	1.46°	3.14°	1.23°
CSQA	1.82°	1.78°	3°	5.28°

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From Table 4.2, the CPQA clearly has the smallest phase error due to component tolerances within a set of attenuators. Even though the double hybrid appears to consistently have the smallest RSS phase error, its true attenuation range is limited due to the PIN diode's complex impedance. For the double hybrid attenuator to achieve an attenuation of 40 dB, the PIN diode impedances have to be 0.25 Ω. The presence of series inductance makes this an unrealistic value.

From all the topologies discussed, the CPQA has the most realistic PIN diode resistance range for a 40 dB dynamic range.

By applying sensitivity analysis to each EVA, it was possible to identify an optimal phase tracking topology with the RSS phase error measure. This novel approach identified the CPQA's phase tracking over control range to have the smallest expected variation. The RSS phase error measure was derived in Chapter 3. Its application to identify an optimal phase tracking set of EVAs is a novel approach, first documented by the author in [53].

The CPQA has not been documented extensively in the available literature, and an analysis of its performance is presented next. The CPQA has an excellent attenuation range and its corresponding PIN diode resistances are within a realistic range (when PIN diode complex impedances are considered). The following analysis is, to the author's knowledge, the first of its kind to document the CPQA in terms of its transmission and reflection coefficient, power dissipation and biasing scheme at L-band.

4.3 CPQA

Using sensitivity analysis and the defined RSS error measure, it was found that the CPQA has optimal phase tracking within a set of attenuators over its full control range.

Apart from the CPQA layout suggested by Walker [32], and attenuation reported in [33], the CPQA's response has not been fully characterised.

Section 4.3.1 shows the CPQA's transmission and reflection coefficients at L-band.

Section 4.3.2 gives a power analysis that determines the amount of power dissipated in each PIN diode. This ensures that the series connected PIN diodes do not exceed their rated power dissipation.

In [33], the CPQA is biased in the center of the two parallel quarter-wave attenuator sections, forcing the current to divide between the two attenuators. By dividing the current, further tolerance errors exist in the PIN diode resistances. A new and improved biasing scheme is proposed in Section 4.3.3, where the PIN diodes are forward biased equally to minimise phase tracking errors.

Fig. 4.9 shows a circuit diagram of the CPQA with a shared bias current source.

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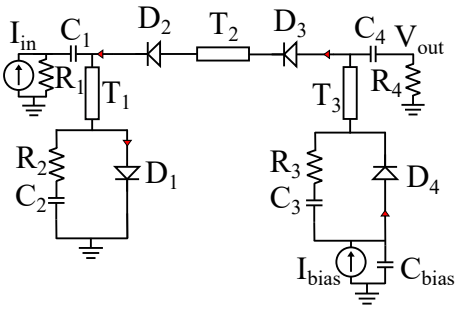
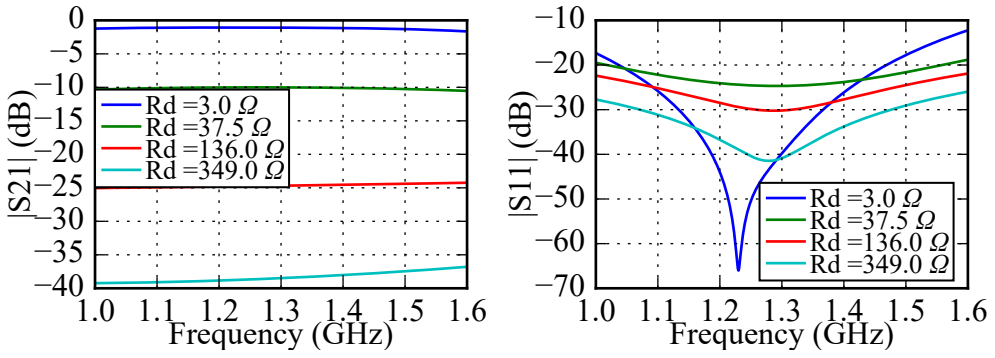


Figure 4.9: CPQA circuit diagram. Current source I_{bias} indicates where DC bias is applied.

4.3.1 Transmission and reflection coefficient

The CPQA's simulated transmission and reflection coefficients are given in Fig. 4.10 for L-band operation.



(a) Transmission coefficient.

(b) Reflection coefficient.

Figure 4.10: Transmission and reflection coefficient of CPQA.

From Fig. 4.10, the CPQA has excellent attenuation flatness over its full control range. Additionally, its reflection coefficient remains below 20 dB for the frequency band $1.2 - 1.4\ GHz$. Another advantage of this topology is the attenuator's compact layout with respect to the amount of attenuation that can be achieved.

For an attenuation range of $<$ 1 dB to 40 dB, the attenuator only requires the PIN diode resistance to vary between 1 Ω and 350 Ω.

4.3.2 CPQA power handling

The temperature increase of each PIN diode's junction is a function of the power dissipated in the diode. A safe operating temperature can be maintained

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by knowing how much power has to be dissipated in each PIN diode and choosing a diode with the appropriate parameters.

Through nodal voltage analysis of the CPQA, it is possible to calculate the power dissipated in each resistive element in the circuit. Fig. 4.11 shows the power dissipated in each PIN diode and resistor in the CPQA, normalised to the input power. The power dissipated in each element is given over PIN diode

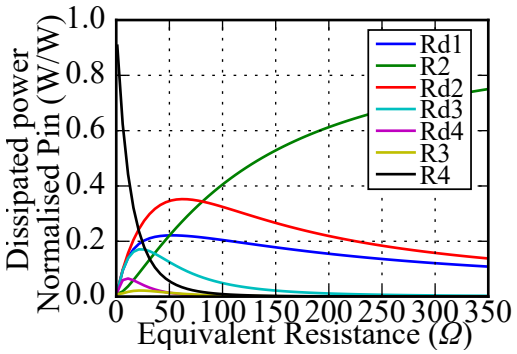

Figure 4.11: Normalised power dissipated versus attenuation for the CPQA. The PIN diodes' resistance is plotted on the X-axis to represent attenuation.

resistance range, the corresponding attenuation range is $< 1\ dB$ to 40 dB.

In Fig. 4.11, R_4 is the load resistance. The series PIN diode D_2 in Fig. 4.9 dissipates the most power when $R_d \approx 50\ \Omega$. The maximum power dissipated in D_2 is only 0.35 times the CW incident power. As a result, the input power can exceed the PIN diodes' rated maximum power dissipation. The parallel 50 Ω resistor R_2 has to be chosen with care, since it dissipates the bulk of the power as attenuation increases.

4.3.3 Analysis of CPQA biasing scheme

Poor isolation between the DC and RF sections often become the limiting factor in a circuit's bandwidth and attenuation range.

In [33], a single bias source is connected to the center of the two back-to-back parallel quarter-wave attenuators, forcing the current to divide between the two sections. By adding possible biasing current variation, the circuit's total output sensitivity to PIN diode impedance variation can increase.

A different biasing structure is presented here wherein all the PIN diodes are biased with the same current. This biasing structure shown in Fig. 4.12 is well isolated from the RF network. In this network, current is applied at the T_7 and C_4 junction.

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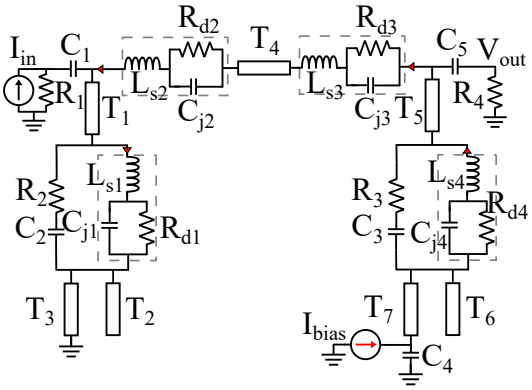

Figure 4.12: CPQA biasing structure. Transmission lines T_3 and T_7 are quarter-wavelength 75 Ω, while T_2 and T_6 are quarter-wavelength 50 Ω lines.

4.3.3.1 Biasing structure design

In Fig. 4.9, a biasing current is applied at diode D_4 and terminates to ground at diode D_1. To isolate the current source from interfering with the RF circuit, quarter-wavelength transmission lines are used.

In Fig. 4.12, a biasing current ($I_{bias} = \frac{V_{bias}}{R_{bias}}$) is applied at transmission line T_7. T_7 is a high impedance quarter-wavelength line that connects to diode D_4's anode. By placing a decoupling capacitor C_4 in parallel with the biasing voltage, T_7 appears as a short circuited transmission line. The quarter-wavelength line transforms the small impedance to an "open circuit" at D_4's anode:

$$|Z_{inbias}| = \frac{|Z_0|^2}{R_{bias}||\frac{1}{|j\omega C_4|}} \tag{4.3.1}$$

To create an RF ground at D_4's anode and further isolate D_4 from Z_{inbias}, an open circuit quarter-wavelength transmission line T_6 is added in parallel with T_7. T_6 becomes an RF short circuit at D_4's anode:

$$|Z_{D4anode}| = (|Z_{inbias}|)||(|Z_{SC}|) \tag{4.3.2}$$

To remove any additional inductance to ground at D_1, a DC ground is constructed by placing the via a quarter-wavelength away from D_1 (T_3). Another open circuit stub (T_2) is placed in parallel with the short circuit stub to ensure an RF ground at D_1. The DC and RF circuits are well isolated from one another.

Clearly a larger characteristic impedance for T_3 and T_7 would result in better isolation, but the characteristic impedance of T_7 and T_3 are constrained by substrate choice and manufacturing capabilities. An impedance of 75 Ω is chosen. The open circuit stubs T_2 and T_6 are chosen to have a characteristic impedance of 50 Ω.

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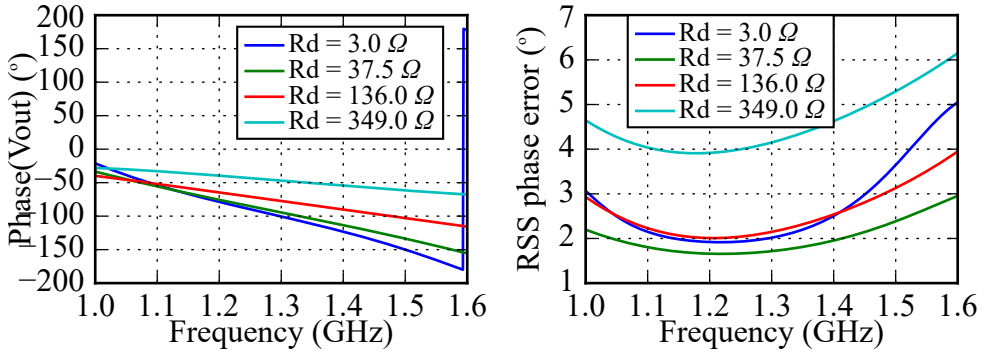
4.3.3.2 Sensitivity analysis of CPQA biasing structure

Sensitivity analysis is applied to Fig. 4.12 to determine the CPQA's output sensitivity to dimensional variations in its biasing transmission lines. The output RSS phase errors over attenuation are calculated for the CPQA with biasing circuitry. The CPQA's transmission phase and RSS phase error are shown in Fig. 4.13.



(a) Transmission phase.

(b) RSS phase sensitivity.

Figure 4.13: CPQA biasing structure with transmission phase and RSS phase error results. Transmission lines T_3 and T_7 are quarter-wavelength 75 Ω, while T_2 and T_6 are quarter-wavelength 50 Ω lines.

Table 4.3 compares the RSS phase error of the CPQA with and without biasing circuitry. From Table 4.3, the total output RSS phase error increases the most when the attenuation is 1 dB.

Table 4.3: Comparing output RSS phase error in degrees of the CPQA with and without biasing circuitry. All values are given at 1.3 GHz.

Attenuation	1 dB	10 dB	25 dB	40 dB
CPQA	1.47°	1.20°	1.90°	4.07°
CPQA with biasing	2.02°	1.72°	2.15°	4.15°

4.3.3.3 Components influencing RSS phase error increase

To find the cause for the increased output RSS phase sensitivity when $R_d = 3\ \Omega$, the output phase sensitivities to variations in transmission line propagation delay is considered here.

The CPQA's transmission phase is given in Fig. 4.14a for $R_d = 3\ \Omega$. The output phase sensitivity to dimensional variation in CPQA transmission lines when $R_d = 3\ \Omega$ is given in Fig. 4.14b. Since the CPQA's layout is symmetrical,

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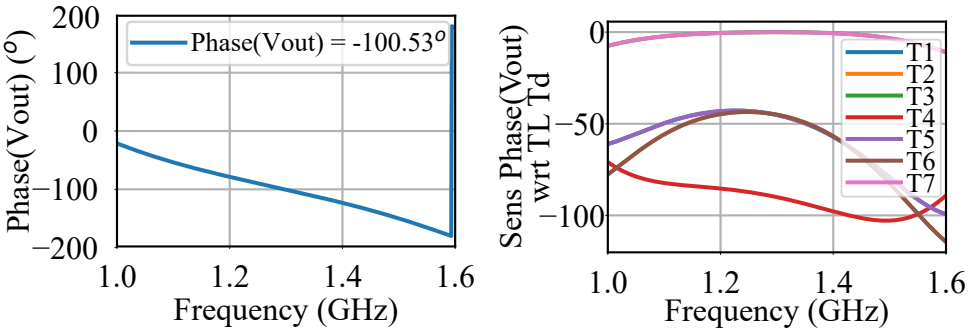
the output phase sensitivities with respect to transmission line propagation delay are equal for $T_7 = T_3$, $T_6 = T_2$ and $T_1 = T_5$.



(a) Transmission phase.

(b) Output phase sensitivity to variations in TL T_d.

Figure 4.14: Individual output phase sensitivity in terms of T_d.

If Fig. 4.14b is considered, T_4 contributes the largest portion of the output phase sensitivity with respect to T_d. Care should be taken to ensure T_4 is manufactured within specification.

From Fig. 4.14b, the output phase is sensitive to variations in T_d of transmission lines T_2 and T_6. By reducing the characteristic impedance of T_2 and T_6, the transmission lines become less sensitive to variations in T_d. This follows from the non-ideal open circuit (Z_{OC}) of T_2 and T_6 that transform to a more ideal short circuit when Z_0 is smaller ($|Z_{in}| = \frac{|Z_0|^2}{|Z_{OC}|}$). However, adjusting Z_0 of T_2 and T_6 might negatively influence the output magnitude or output RSS phase error.

Table 4.4: Comparing output RSS phase error of the CPQA with and without biasing circuitry. Additionally, output RSS phase error is given when $Z_{T_2} = Z_{T_6} = 25\ \Omega$. All RSS phase errors are given at 1.3 GHz.

Attenuation	1 dB	10 dB	25 dB	40 dB
CPQA	1.47°	1.20°	1.90°	4.07°
CPQA with biasing	2.02°	1.72°	2.15°	4.15°
CPQA with biasing $Z_{T_2} = Z_{T_6} = 25\ \Omega$	1.74°	1.45°	2.00°	4.10°

The RSS phase error results of a simulation with Z_0 of T_2 and T_6 equal to 25 Ω is given in Table 4.4. The final CPQA was implemented with Z_0 of T_2 and T_6 equal to 50 Ω.

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Individual output and input voltage sensitivity results give a unique insight into the CPQA's operation.

4.3.4 CPQA implementation

A maximum power of 250 mW can be dissipated in the BAR50-2 PIN diode. From the maximum power dissipation calculations this translates to a maximum CPQA input power of 714 mW CW.

By including the biasing network in the sensitivity analysis of the CPQA, it was possible to identify and adjust the components that increased the CPQA's phase tracking error. This novel approach to phase tracking design results in improved performance and allows the identification of an optimal layout.

A set of six CPQAs are manufactured and measured in the following sections. The measured phase of a set of CPQAs is compared to the simulated RSS phase error over control range.

4.4 Vector network analyser set-up and phase tracking calibration

Measuring the CPQA has two goals:

1. Measure the phase tracking of a set of six CPQAs.
2. Compare the measured transmission and reflection coefficients to simulated values.

To accurately measure the phase tracking of a set of CPQAs, the measurement set-up's phase error has to be considered.

The set-up used to measure the set of EVAs is given in Fig. 4.15.

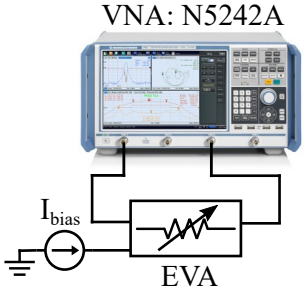

Figure 4.15: Test set-up to measure small signal parameters and phase tracking of a set of CPQA.

The VNA's phase error over varying transmission coefficient has to be smaller than the expected RMS phase error of the CPQA over control range.

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The VNA set-up is used to measure both a set of CPQAs' phase tracking and the transmission and reflection coefficients of a CPQA.

4.4.1 Vector network analyser accuracy

Calibrating the *N5242A* VNA from *Keysight* with ECal *N4691B*, the VNA's transmission phase measurement variation is shown in Fig. 4.16. Over the

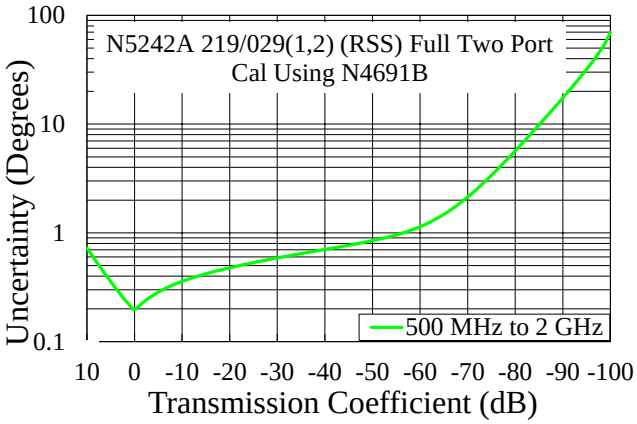

Figure 4.16: VNA phase accuracy [54].

CPQA's full control range, in the worst case the VNA will add less than 0.7 ^{o} to the measured phase error. The VNA will not contribute the dominating phase error during RSS phase error measurements. The phase uncertainty in Fig. 4.16 is valid for an ambient temperature between $20-30\ ^oC$. To maintain an accurate calibration during measurements, the ambient temperature should not vary by more than 1 ^oC [55].

Six CPQAs are manufactured with the goal of measuring their phase tracking over control range. The six CPQAs are measured between 1 dB and 40 dB. Phase stable cables are used for the measurement. The cables are kept in the same position for each measurement.

4.4.2 CPQA implementation

The CPQA is implemented on Rogers RO4003 with a substrate height of 0.508 mm. The substrate height is dictated by the limiter from Chapter 5. Fig. 4.17 shows a photo of six manufactured CPQAs. Panel mount SMA connectors are used as is seen in Fig. 4.17. However, the panel mount SMA connectors resulted in a large transition mismatch to the microstrip circuit. The reflection coefficient of the SMA connectors are approximately 20 dB. Two through lines are used to measure the SMA transition, the results are given in Fig. 4.18. Fig. 4.18c shows the transmission phase of the two through

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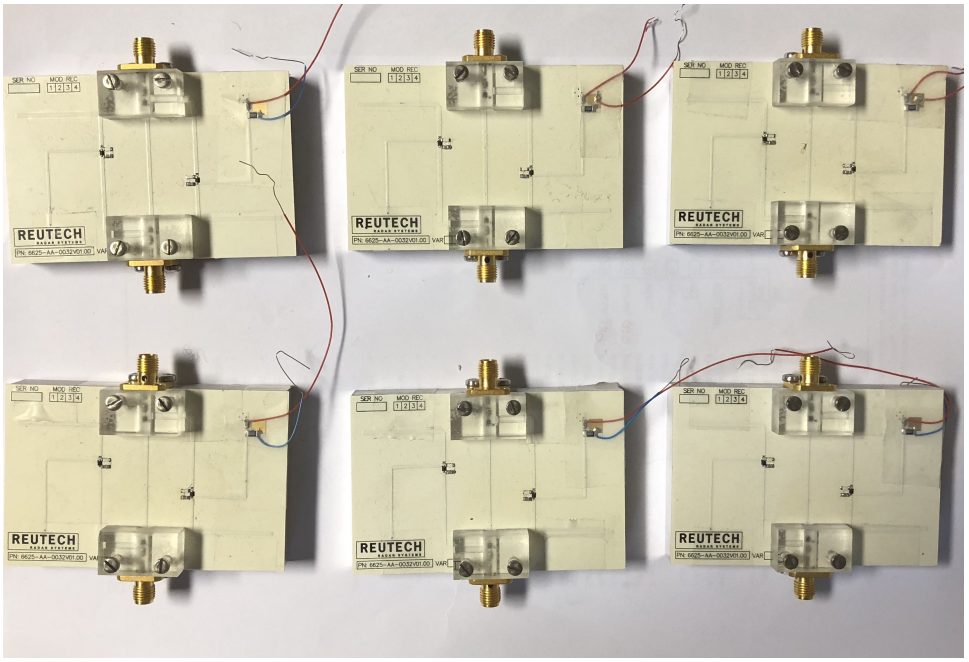

Figure 4.17: Photo of manufactured set of CPQAs.

lines. The phase difference between the two lines is less than 1 ^{o} over the frequency band $1.2 - 1.4\ GHz$. The phase error added by the SMA connector mismatches will not be the dominant error during the EVA phase tracking measurements.

The VNA has sufficient accuracy to measure the phase tracking performance of a set of CPQAs. The reflection coefficient of the CPQA measurements will be degraded slightly by the SMA transitions. However, it was found that the reduced reflection coefficient will not negatively influence the expected phase tracking.

Extreme care was taken to ensure the repeatability of the measurements.

4.5 Measurements

Two sets of measurements are given for the CPQA. Firstly, a single CPQA's transmission and reflection coefficients are measured over the control range. Next, the transmission phase of six CPQAs are measured over the control range and compared to the calculated RSS phase error.

4.5.1 Transmission and reflection coefficient

A single CPQA's measured transmission and reflection coefficients are given in Fig. 4.19 for L-band. The desired band of operation is $1.2 - 1.4\ GHz$.

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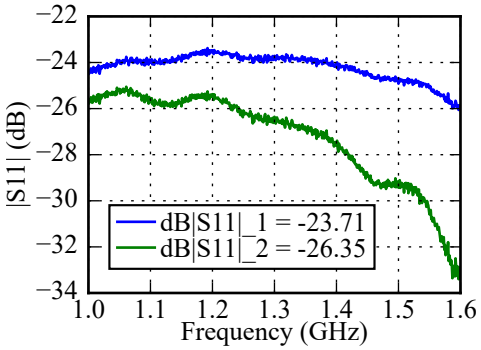
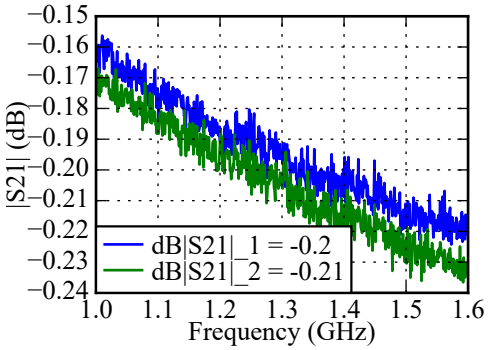
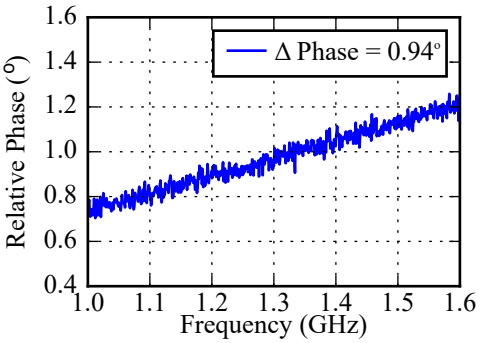


(a) Reflection coefficient.

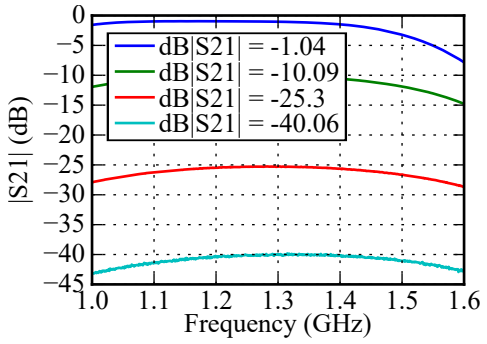


(b) Transmission coefficient.

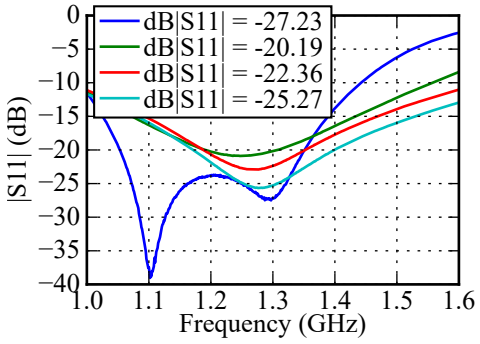


(c) Transmission phase.

Figure 4.18: Two calibration lines used to measure SMA reflection and transmission coefficient. The unwrapped phase difference of the two calibration lines is given in Fig. 4.18c



(a) Transmission coefficient.



(b) Reflection coefficient.

Figure 4.19: Measured transmission and reflection coefficients of a single CPQA. The frequency band of interest is between $1.2 - 1.4\ GHz$. The results are displayed in the legend from top to bottom for $R_d = 3\ \Omega, 37.5\ \Omega, 136\ \Omega, 349\ \Omega$.

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Consider the measured $|S_{21}|$ in Fig. 4.19a: at the edges of the frequency band the attenuation flatness degrades more than in the simulated case. Further investigation of the CPQA's output magnitude sensitivity in terms of transmission line T_d reveals that there is an increase in output sensitivity at the edges of the frequency band. However, at the center frequency the CPQA's $|S_{21}|$ behaves as expected.

The measured reflection coefficient in Fig. 4.19b is also different from the simulated results, most notably when $R_d = 3\ \Omega$. Additional capacitance to ground and series inductance due to step transitions cause variation to the impedance seen by the input. The reflection coefficient of the SMA transition also degrades the total reflection coefficient.

The measured attenuation flatness over the band $1.2 - 1.4\ GHz$ is given in Table 4.5.

Table 4.5: Measured CPQA attenuation flatness over attenuation range for 1.2 GHz to 1.4 GHz.

Attenuation	1 dB	10 dB	25 dB	40 dB
Attenuation flatness (dB)	0.52 dB	0.52 dB	0.36 dB	0.26 dB

The CPQA has excellent measured transmission and reflection coefficients in the desired frequency band ($1.2 - 1.4\ GHz$).

4.5.2 Measured phase tracking of a set of CPQAs

Six CPQAs were measured for ideal $L = 1, 10, 25, 40\ dB$. The unwrapped transmission phase of each CPQA is given relative to the unwrapped transmission phase of CPQA 1. The difference in unwrapped transmission phase is shown in Fig. 4.20. The phase tracking decreases significantly in the band where the reflection coefficient is below 10 dB.

According to Fig. 4.16, the phase measurement error increases as the transmission magnitude decreases. The VNA measurement error also increases as S_{21} becomes smaller.

Table 4.6 summarises the measured RSS phase error of a set of CPQA over control range. All the measured RSS phase errors are smaller than the

Table 4.6: Maximum measured phase variation at 1.3 GHz between a set of CPQA.

Attenuation	1 dB	10 dB	25 dB	40 dB
RSS phase error (max)	0.49 ^{o}	0.72 ^{o}	1.18 ^{o}	1.58 ^{o}

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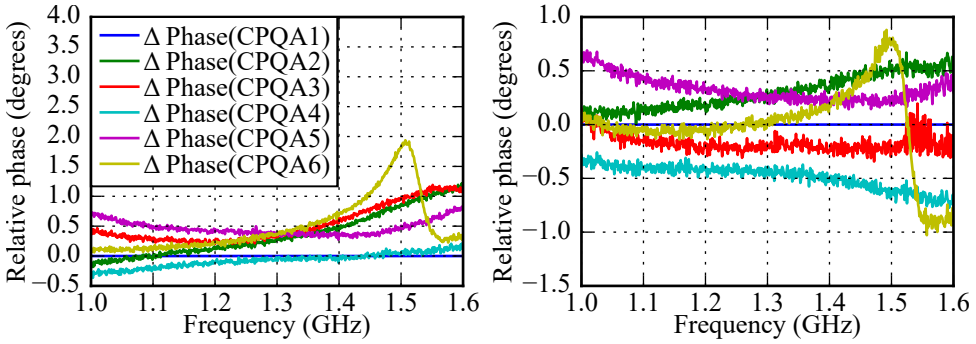
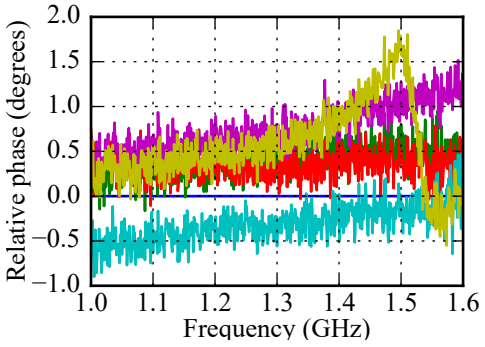
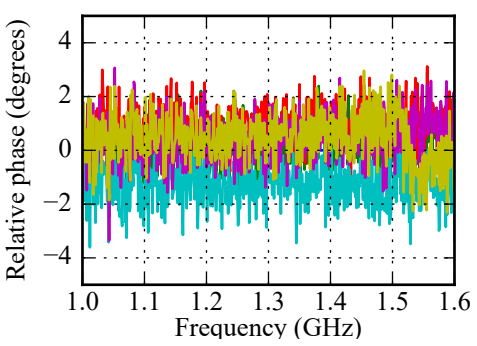


(a) 1 dB attenuation.

(b) 10 dB attenuation.



(c) 25 dB attenuation.



(d) 40 dB attenuation.

Figure 4.20: Relative transmission phase of six CPQAs for $L = 1, 10, 25, 40\ dB$. The unwrapped transmission phase of CPQAs 2 to 6 are subtracted from the unwrapped transmission phase of CPQA 1. The legend in Fig. 4.20a is also applicable to Figs. 4.20b to 4.20d.

predicted RSS phase error. However, the increase in RSS phase error as attenuation increases is similar to the predicted values.

Through measurements it was confirmed that the CPQA has optimal phase tracking within a set of CPQAs.

4.6 Conclusion

For good phase tracking in a multi-channel receiver, the set of EVAs providing STC have to track in phase. Variations in the complex PIN diode impedance and other component variations cause phase tracking errors in a set of attenuators.

An RSS phase error measure was defined in Chapter 3. By calculating the RSS phase error of several matched attenuators, it was possible to identify a topology with optimal phase tracking.

The parallel quarter-wave attenuator had good phase tracking results for low attenuation. However, its RSS phase error increased as its PIN diode

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resistance increased. Additionally, it was not matched at its output port over the full control range. By viewing the individual phase sensitivity results of the parallel quarter-wave attenuator, it was found that its series PIN diode's junction capacitance caused the output phase error to increase with increasing PIN resistance R_d. Cascading two of these topologies back-to-back, the output phase dependence on the series PIN diode's junction capacitance could be minimised. The new cascade parallel quarter-wave attenuator (CPQA) had a low RSS phase error over control range.

Comparing the RSS phase error of the chosen matched attenuators, the CPQA was identified as an attenuator with optimal phase tracking in set of EVAs. Once the CPQA was identified as the optimal phase tracking topology, further analyses was performed on the circuit.

The CPQA's transmission and reflection coefficients were simulated for L-band, and the power dissipated in each PIN diode over attenuation was calculated. An improved biasing structure was proposed for the CPQA that allowed all four PIN diodes to be forward biased equally.

It was found that the CPQA had optimal phase tracking within a set of attenuators, excellent attenuation flatness, attenuation range, it was matched over the full attenuation range, it was a compact structure and it used only a single biasing feed.

The CPQA's exceptional performance was documented with measurements where six CPQAs showed phase tracking errors that were between 0.4 ^{o} and 1.2 ^{o} at the center frequency over a 40 dB attenuation range.

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Chapter 5

Compact High Power Limiter

5.1 Introduction

Fig. 5.1 shows a single channel of a multi-channel radar front end. An antenna is connected to a transmitter and receiver through a circulator. If the antenna has a poor reflection coefficient, a large portion of the transmitted power is reflected to the receiver during each transmit cycle. As an example, if the

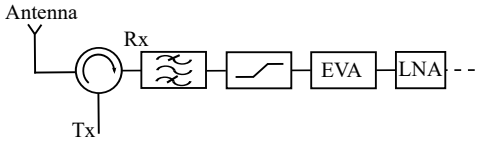

Figure 5.1: Transmitter/Receiver with an antenna and circulator.

transmitted pulse has a peak power of 1 kW (60 dBm), an antenna reflection coefficient of 10 dB will result in a reflected power of 100 W (50 dBm) incident on the receiver. The receiver in Fig. 5.1 needs protection from large reflections during the transmit cycle.

In Chapter 2, the three operation modes of a limiter were discussed: active, passive and quasi-active.

1. In active mode, large synchronous signals are blocked by externally biasing the limiter during the transmit cycle. The transmitter's trigger signal can be used to enable a biasing current that switches the limiter on and off.

2. In passive mode, large non-synchronous signals in the radar's band are limited through self-biased PIN diodes. A self-biased PIN diode is either a PIN diode with a parallel connected inductor, or an anti-parallel connected PIN and Schottky diode.

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3. In quasi-active mode, a limiter can protect a receiver both synchronously and non-synchronously. By using a coupler where the coupled port connects a Schottky diode to the limiter's PIN diode, the Schottky diode is driven directly by the input signal. Since the Schottky diode is directly driven by the input signal and not influenced by the PIN diode's decreasing impedance, the Schottky diode is quasi-actively driving the PIN diode.

In Chapter 5, a limiter that operates in both active and passive mode is developed. This configuration will be referred to as an **active PIN-Schottky limiter**.

For the limiter developed in this dissertation, active mode protects the receiver mainly from the radar's transmitted signal reflecting from the antenna. The limiter's passive mode protects the receiver from close range target reflections, and other radars transmitting in the same band. For the application demonstrated in Fig. 5.1, the limiter's passive mode's power handling requirement is lower than that for the active mode.

A PIN diode limiter's power handling depends on how much its junction temperature increases as power is dissipated in the junction. To determine the power dissipated in a PIN diode, the diode's minimum resistance has to be known.

For commercially available PIN diodes, datasheets often give the resistance for only a single forward current. The datasheet resistance is a combination of the PIN diode's N layer and bond wire resistance plus the I region resistance at the given forward current. The problem is that manufacturers do not specify bond wire, and N and P layer resistances. Insufficient information regarding the PIN diode's minimum attainable resistance makes it difficult to estimate how much power is dissipated in the diode during high power operation.

Finding the PIN diode's minimum attainable resistance is crucial to determine the maximum input power that the limiter can safely handle. Using a small signal measurement to find the resistance offers its own challenges. From the PIN diode small signal model discussed in Chapter 2, the PIN diode's package adds a small series inductance to the diode's impedance. The presence of series inductance makes it difficult to reliably measure the minimum resistance with a small signal measurement on a vector network analyser (VNA).

This chapter describes a large signal method to determine a PIN diode's resistance under heavy forward bias.

The design of an active PIN-Schottky limiter is discussed in Section 5.2. Sensitivity analysis is used to optimise the limiter's small signal response. Furthermore, a simple improvement to the limiter's layout is given that significantly improves its passive reverse recovery time.

Small and large signal simulation results of the designed limiter are given in Section 5.3.

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The limiter's measurements are given in Sections 5.4 and 5.5. First, the limiter's small and passive large signal measurements are given in Section 5.4. These are referred to as the characterising measurements. Second, the limiter's high power active measurements are performed and documented in Section 5.5.

For the active measurements in Section 5.5, the 'coarse' PIN diode is calibrated in terms of diode voltage versus junction temperature. As the PIN diode's junction temperature increases, its voltage decreases [6]. By knowing the slope of this change, the junction temperature can be monitored while increasing the input power during high power measurements.

In Section 5.5, the PIN diode's voltage response to a high power input is compared with the thermal simulation results discussed in Section 5.3. By comparing measured and simulated junction temperature increase, the PIN diode's resistance is estimated.

5.2 Design

The design of an active PIN-Schottky limiter is described in this section.

The limiter is actively biased during the radar's transmit cycle, and creates an impedance mismatch that reflects incident power. If the limiter is not actively biased, it can still operate in passive mode. When an unexpected large signal is incident on the receiver, the limiter self-biases and reflects a portion of the received signal.

The active PIN-Schottky limiter layout is discussed in Section 5.2.1.

Section 5.2.2 gives the criteria for PIN and Schottky diodes, followed by a list of diodes that are commercially available.

In Section 5.2.3, Sensitivity analysis from Chapter 3 is used to optimise the limiter's input reflection coefficient. Improving a limiter's reflection coefficient is challenging. The junction capacitance of PIN and Schottky diodes are dependent on available components, making many component choices a trade-off between insertion loss, better reflection coefficient and limiting performance. By using manual optimisation, it is possible to use available PIN and Schottky diodes to find a good reflection coefficient for the limiter. The approach discussed in Section 5.2.3 enables a more intuitive process that identifies components that are sensitive to variation and choose the most appropriate components for reflection coefficient without lengthy trial and error.

5.2.1 Layout

5.2.1.1 Passive limiter

Fig. 5.2 shows a two-stage passive limiter where Schottky diodes D_2 and D_4 are connected in anti-parallel with PIN diodes D_1 and D_3. Schottky diodes are used to replace a parallel inductor to lower the limiter's input 1 dB compression threshold and decrease turn-on time.

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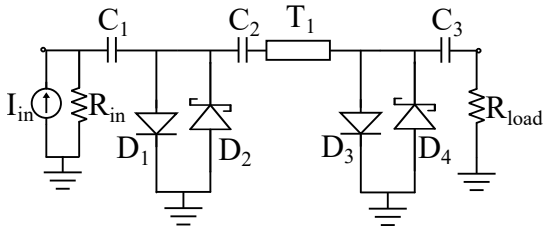

Figure 5.2: Passive limiter circuit diagram. D_1 and D_3 are PIN diodes, D_2 and D_4 are Schottky diodes. T_1 is a quarter-wavelength transmission line at the center frequency with $Z_0 = 50\ \Omega$.

The first PIN diode (D_1) in Fig. 5.2 is known as the 'coarse' diode, and will have to handle the bulk of the power. D_3 is the 'clean-up' diode and determines the flat leakage of the limiter. Typically, PIN diode D_3 has a lower I region width (a lower turn on threshold) and turns on faster than the 'coarse' limiter diode D_1. T_1 is a quarter-wavelength transmission line at the center frequency, with a 50 Ω characteristic impedance. As the second PIN diode turns on, a standing wave is created on the quarter-wavelength line. The standing wave creates a maximum at D_1, decreasing D_1's turn-on time. PIN diodes D_1 and D_3's turn on thresholds are lowered by the Schottky diodes D_2 and D_4.

5.2.1.2 Active PIN-Schottky limiter

Fig. 5.3 shows an active PIN-Schottky limiter. For active operation, D_1

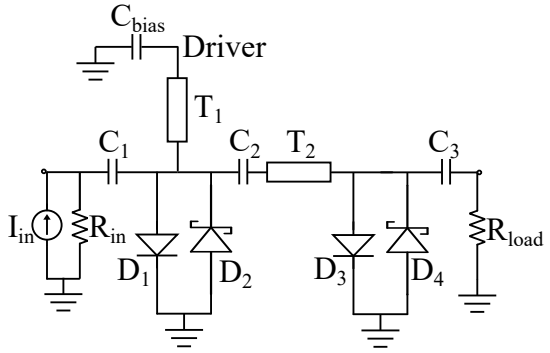

Figure 5.3: Active PIN-Schottky limiter circuit diagram. T_1 is a quarter-wavelength transmission line at the center frequency with $Z_0 = 75\ \Omega$. D_1 and D_3 are PIN diodes, D_2 and D_4 are Schottky diodes. T_2 is a quarter-wavelength transmission line at the center frequency with $Z_0 = 50\ \Omega$.

has to be forward biased synchronously with the transmit cycle. A quarter-wavelength line (T_1) is used to apply a DC current to D_1. The bypass capacitor

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C_{bias} has a small impedance at the center frequency. The biasing circuitry connected through T_1 to D_1 is isolated from the RF section. The impedance of the biasing line seen by D_1 is large as long as $|Z_C|$ is small:

$$|Z_{in}| = \frac{Z_0^2}{|Z_C|} \tag{5.2.1}$$

where $|Z_C| = \frac{1}{|j2\pi f C_{bias}|}$. From Eq. 5.2.1 it is clear that a higher characteristic line impedance for T_1 results in better isolation. It is important to note that the charge stored in an unnecessarily large C_{bias} will slow the PIN diode's recovery time.

5.2.1.3 Proposed reverse recovery time improvement

Consider again the active PIN-Schottky limiter in Fig. 5.3. When the limiter is operating in its passive mode, Schottky diode D_2 closes the DC current path that allows PIN diode D_1's I region to fill with charge and lower its I region resistance. Once the large incident signal has passed, the charge in the PIN diode does not dissipate immediately.

The I region maintains its charge, and as a result, its forward voltage, until the charge in the I region has been removed. In a PIN-Inductor limiter, the PIN diode's voltage over the inductor causes a current to flow out of the PIN diode. However, with the Schottky diode in place of an inductor there is no DC current path through which a reverse current can flow. When charge is dissipated in the I-region through recombination only, the reverse recovery time of a passive limiter is much slower than the PIN diode's minority carrier lifetime.

In Chapter 2, a PIN diode's recovery time from forward biased to reverse biased operation was given as:

$$\tau_{FR} = \tau_L \log_e(1 + \frac{I_f}{I_R}) \tag{5.2.2}$$

where τ_{FR} is the time it takes the PIN diode to move from forward to reverse biased mode, τ_L is the PIN diode's minority carrier lifetime, I_f is the forward current that was applied and I_R is the reverse current. When no reverse current is applied, I_R is the reverse leakage current of the Schottky diode. From Eq. 5.2.2, the reverse recovery time is dependent on the PIN diode's minority carrier lifetime. However, recovery time can be increased or decreased depending on the reverse current applied to the diode.

An improvement is made to the active PIN-Schottky limiter's reverse recovery time in this dissertation.

By adding a resistor in parallel with C_{bias}, a discharge path is created for the charge stored in PIN diode D_1. The value of the resistor is a trade-off between how fast the reverse recovery time should be and current division between the PIN diode and the added resistor during active operation.

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In active operation, the biasing current will divide between the PIN diode and the resistor. As long as the resistor is large enough, this should have minimal effect.

Fig. 5.4 shows the final circuit diagram of the limiter, where a reverse recovery resistor of 1 $k\Omega$ is chosen.

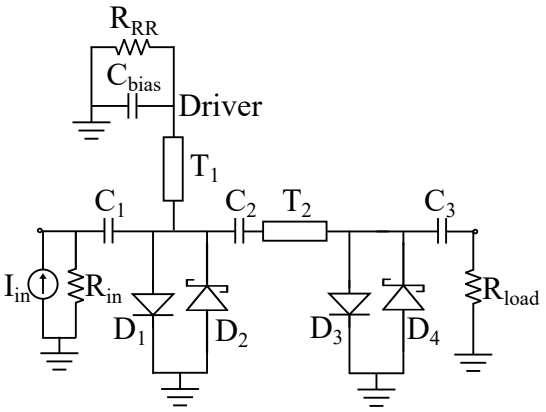

Figure 5.4: Active PIN-Schottky limiter circuit diagram. T_1 is a quarter-wavelength transmission line at the center frequency with $Z_0 = 75\ \Omega$. D_1 and D_3 are PIN diodes, D_2 and D_4 are Schottky diodes. T_2 is a quarter-wavelength transmission line at the center frequency with $Z_0 = 50\ \Omega$. $R_{RR} = 1\ k\Omega$.

5.2.2 Components

The active PIN-Schottky limiter discussed in the previous section requires two PIN diodes and two Schottky diodes.

A quick discussion of PIN diodes is given in the subsequent subsection, followed by a list of available PIN diodes. In the next subsection, Schottky diode requirements are reviewed and the available Schottky diodes are given.

5.2.2.1 PIN diodes

The criteria for surface mount PIN diode selection are:

1. Low junction capacitance (C_j).
   A low junction capacitance improves the limiter's small signal match. It is possible to embed the junction capacitance in a low pass filter structure to reduce its effects.

2. Low resistance ($R_s + R_d$) where R_s is the combination of bond wire, N and P layer resistances, and $R_d = R_d(Imax)$.
   The PIN diode's resistance is typically specified as a single value at a particular forward current. This makes it difficult to gauge what the PIN

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diode's resistance is when a large forward current is applied ($Imax$). The minimum attainable resistance is a crucial parameter that determines how much power is dissipated in the PIN diode:

$$P_d = P_L \frac{4(R_s + R_d(Imax))}{Z_0} \tag{5.2.3}$$

where P_L is the applied power, P_d is the power dissipated in the PIN diode and Z_0 is the characteristic impedance. R_d is limited by the maximum current that flows through the PIN diode ($Imax$). The above equation differentiates between the PIN diode's adjustable I region resistance R_d and the resistance R_s contributed by copper, bond wires and most significantly the PIN's N-layer. R_d might be adjustable to extremely small values, but if R_s is large, the PIN diode's power handling ability will be limited.

3. Good thermal conductivity (Low θ_{jc})
   PIN diodes are specified with a thermal resistance (junction-case) θ_{jc} given in $^oC/W$. The thermal resistance relates the PIN diode's junction temperature increase for CW power dissipated in the junction.

   For a surface mount PIN diode, the thermal resistance of the complete heat removal path from the PIN diode's junction to ambient has to be included in the calculation.

4. Low carrier lifetime (τ_L)
   The PIN diode's carrier lifetime determines its reverse recovery time in passive operation. A smaller τ_L results in faster reverse recovery, allowing the timely detection of target signals that follow the limiting operation.

5. Appropriate reverse breakdown voltage
   Ensure that the largest signal incident on any given PIN diode does not exceed the diode's breakdown voltage.

Table 5.1 lists plastic packaged PIN diodes that were considered for the design's 'coarse' PIN diode.

Table 5.1: Available plastic packaged PIN diodes.

	W (μm)	$C_j(pF)$	$(R_s + R_d)@I_f$	θ_{jc}	τ_L
MADL-011023		0.2	1.3 Ω	175 $^oC/W$	100 ns
MPL7120-2012	10 μm	0.3	1 Ω @ 10 mA	45 $^oC/W$	50 ns
CLA4608-085LF	7 μm	0.65	1.2 Ω @ 10 mA	29 $^oC/W$	100 ns
CLA4609-086LF	20 μm	0.6	1.5 Ω @ 10 mA	25 $^oC/W$	1.1 μs
CLA4611-085LF	12 μm	0.35	1.2 Ω @ 10 mA	15 $^oC/W$	300 ns

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For the 'clean-up' diode, the criteria remain the same. However, additional criteria include:

1. The I region width has to be smaller than the 'coarse' PIN diode.
2. The PIN diode's carrier lifetime has to be much shorter than the 'coarse' PIN diode.

Table 5.2 gives some examples of PIN diodes that can be used as the 'clean-up' diode. For this design, the *CLA4611* and *CLA4606* are chosen as 'coarse' and

Table 5.2: Available plastic packaged PIN diodes for the 'clean-up' diode.

	W (μm)	$C_j(pF)$	$(R_s + R_d)@I_f$	θ_{jc}	τ_L
CLA4608-085LF	7 μm	0.65	1.2 Ω @ 10 mA	29 $^oC/W$	100 ns
CLA4610-085LF	4.5 μm	0.35	2.2 Ω @ 10 mA	73 $^oC/W$	20 ns
CLA4606-085LF	2.5 μm	0.38	2 Ω @ 10 mA	91 $^oC/W$	15 ns

'clean-up' diodes, respectively.

5.2.2.2 Schottky diodes

Two Schottky diodes are needed, the general criteria for a PIN limiter's Schottky diode are:

1. Large enough breakdown voltage (V_b)
   The breakdown voltage of the first PIN diode's Schottky diode has to be larger than the voltage leaking past the 'coarse' PIN diode. The leaked voltage depends on the maximum expected input power and the minimum resistance of the PIN diode. The second PIN diode's Schottky diode breakdown voltage requirement is much lower, since the bulk of the power is handled by the first PIN diode.
2. Small series resistance (R_s) and low barrier voltage (V_f)
   The Schottky diode's series resistance and barrier voltage are considered together. A lower forward voltage will allow the Schottky diode to start conducting current at a lower input voltage. A low series resistance results in more current injected into the PIN diode initially, increasing its passive turn-on time.
3. Small junction capacitance (C_j)
   A small junction capacitance helps to maintain a good input and output match. For optimal reflection coefficient performance, PIN and Schottky diode capacitances should be selected carefully. This is discussed further in the next section.

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Table 5.3: Available surface mount Schottky diodes. 'N.G.' refers to parameters that were not given on the datasheet.

	V_b	R_s	V_f	C_j
1N5711W-7-F	70 V	N.G.	0.41 V	2 pF @ 0V
HSMS-2800-TR1G	70 V	35 Ω	0.41 V	2 pF @ 0 V
MMBD770T1G	70 V	N.G.	0.42 V	1 pF @ 20 V
SMS3924	70 V	11 Ω	0.49 V	1.43 pF @ 0 V
SMS3925	40 V	5.4 Ω	0.62 V	0.48 pF @ 0 V
MAAL2505	5 V	10 Ω	0.3 V	0.1 pF @ 0 V

Table 5.3 lists the available Schottky diodes. For this design, the *SMS3925* is chosen as the 'coarse' PIN diode's Schottky diode and *MAAL2505* is chosen for the 'clean-up' PIN diode's Schottky diode.

5.2.3 Small signal S_{11} sensitivity

Sensitivity analysis of the limiter's small signal model is used to optimise the limiter's reflection coefficient. Considering the sensitivity of the reflection coefficient to component variations, the components in the limiter can easily be changed to find a better input match. Automatic optimisation does not offer the same insight that is gained from using this method. By using a manual optimisation approach, it is possible to identify the areas in the circuit that are the most sensitive to component variation.

This section describes the derivation of S_{11} magnitude and phase sensitivity to variations in lumped and distributed components.

Fig. 5.5 gives a simplified small signal model of the active PIN-Schottky limiter. The Schottky diodes appear as shunt capacitors in their reverse biased

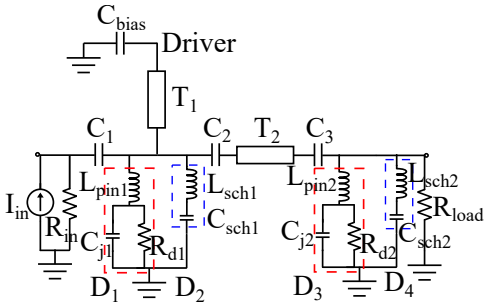

Figure 5.5: Small signal model of active PIN-Schottky limiter.

operation. For this example, T_2 is a quarter-wavelength 50 Ω transmission line at the center frequency, T_1 is a quarter-wavelength 75 Ω transmission line at the center frequency, $L_{pin1} = 0.1\ nH$, $C_{j1} = 0.35\ pF$, $R_{d1} = 1\ k\Omega$, $L_{sch1} = 0.1\ nH$,

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$C_{sch1} = 0.48\ pF$, $L_{pin2} = 0.1\ nH$, $C_{j2} = 0.35\ pF$, $R_{d2} = 1\ k\Omega$, $L_{sch2} = 0.1\ nH$, $C_{sch2} = 0.48\ pF$.

The input reflection coefficient is related to the input voltage by:

$$S_{11} = V_{in} - 1 \tag{5.2.4}$$

This equation holds true when a source is applied at the input with a $2\ V$ open circuit voltage. The partial derivative of the reflection coefficient in terms of the input voltage is:

$$\frac{\partial S_{11}}{\partial V_{in}} = 1 \tag{5.2.5}$$

The sensitivity of the input reflection coefficient to variation in component values can now be calculated for k elements using:

$$S_{g_k}^{S_{11}} = S_{g_k}^{V_{in}} \frac{\partial S_{11}}{\partial V_{in}} \frac{V_{in}}{S_{11}} \tag{5.2.6}$$

From Chapter 3, the change in S_{11} phase due to component g_k variation is calculated using:

$$\Delta\angle S_{11} \approx \mathrm{Im}\left(S_{g_k}^{S_{11}}\right) \frac{\Delta g_k}{g_k} \tag{5.2.7}$$

and the change in S_{11} magnitude to variation in component g_k:

$$\frac{\Delta|X_{out}|}{|X_{out}|} \approx \mathrm{Re}\left(S_{g_k}^{Y_{out}}\right) \frac{\Delta g_k}{g_k} \tag{5.2.8}$$

The steps below are used together with an example to improve the reflection coefficient of the limiter in Fig. 5.5. When using the method described below, care should be taken to consider all corresponding output magnitude or phase sensitivities of the component that was changed.

1. **Use S_{11} phase sensitivities to small variations in transmission line T_d to identify the best input match at the desired frequency.**

   Consider the Smith chart of S_{11} in Fig. 5.6a, where the reflection coefficient crosses the real axis approximately when $f_0 = 1.3\ GHz$. This observation is confirmed by the phase of S_{11} in Fig. 5.6b where $\mathrm{Phase}(S_{11}) = 7.91^o$ at $f_0 = 1.3\ GHz$.

   The best match exists where the reflection coefficient is the closest to the center of the Smith chart. From the Smith chart in Fig. 5.6a, it is clear that the circuit in Fig. 5.5's best match is not at $1.3\ GHz$.

   From the reflection coefficient magnitude in Fig. 5.7a, the best match occurs at $1.26\ GHz$. This corresponds to the Smith chart in Fig. 5.6a.

   The reflection coefficient's sensitivity to variations in transmission line T_d is given in Fig. 5.7b. By varying T_d, the phase of the reflection coefficient

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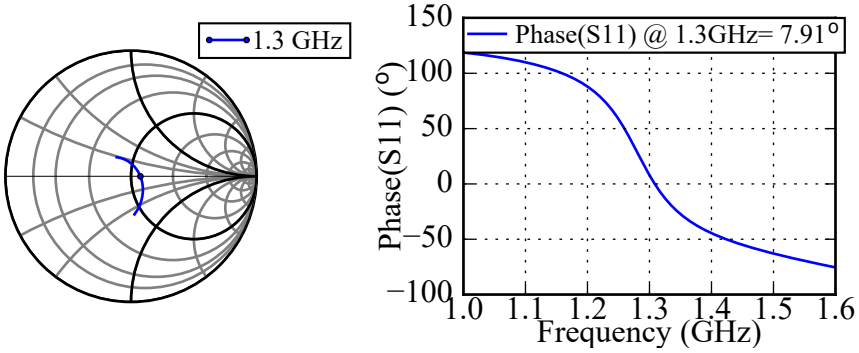
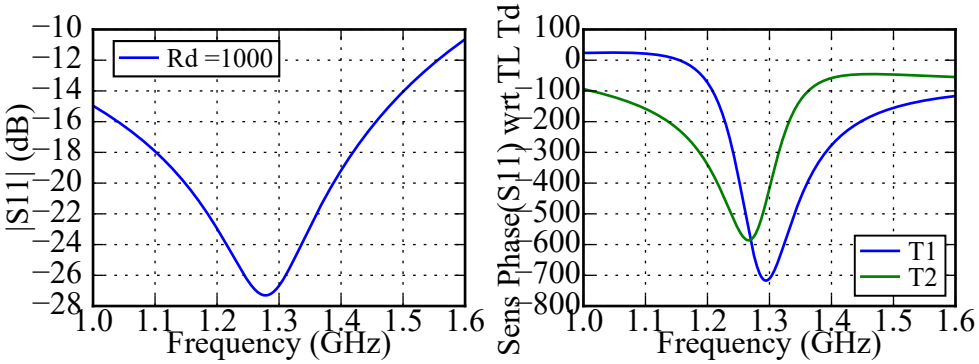


(a) Reflection coefficient on Smith chart. (b) Reflection coefficient phase.

Figure 5.6: Limiter reflection coefficient given on the Smith chart. The reflection coefficient's phase is also given to show its zero crossing.



(a) Reflection coefficient magnitude. (b) S_{11} phase sensitivity with respect to TL T_d in degrees (^{o}).

Figure 5.7: Limiter reflection coefficient magnitude and phase. Plotting S_{11} on the Smith chart shows how adjusting S_{11} phase will change the frequency crossing the real axis.

in Fig. 5.6b can be adjusted to move the optimal match position around in frequency. Changing the reflection coefficient's phase in the desired direction corresponds to moving the plot on the Smith chart in Fig. 5.6a in a counter clockwise direction.

If S_{11}'s phase sensitivity with respect to transmission line T_d is considered in Fig. 5.7b, changing the propagation delay of T_1 will change the phase response of S_{11}. Assuming that the magnitude of S_{11} is insensitive to T_1 propagation delay variations, Eq. 5.2.7 is used to calculate the change in propagation delay needed to shift the phase at 1.3 GHz to the phase at

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1.26 GHz:

$$\Delta T_d \approx T_d \frac{\Delta \angle S_{11}}{\mathrm{Im}\left(S_{T_d}^{S_{11}}\right)} \approx -7\ ps \tag{5.2.9}$$

2. **Adjusting T_d will affect S_{11} magnitude.**
   Consider the uncompensated S_{11} magnitude sensitivity in terms of transmission line T_d in Fig. 5.8. Changing T_1's propagation delay reduces the

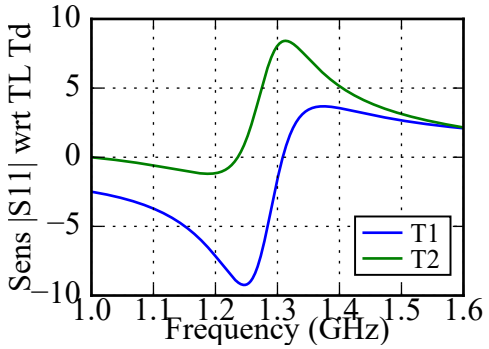
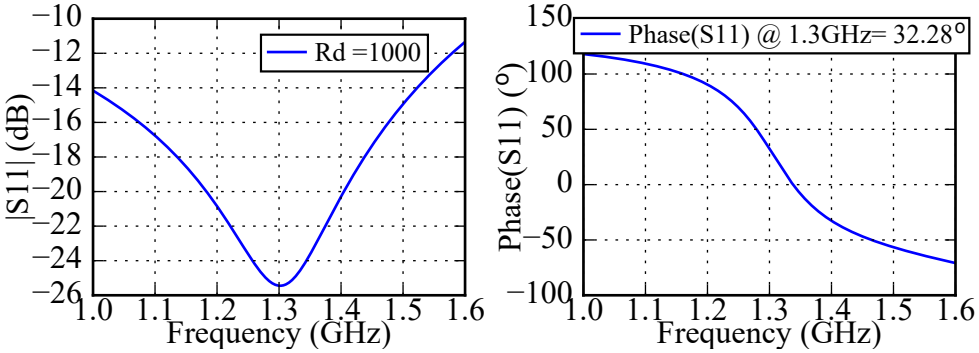


Figure 5.8: S_{11} magnitude sensitivity with respect to transmission line T_d.

reflection coefficient magnitude as seen in Fig. 5.9a.

Using the rest of the limiter's S_{11} magnitude sensitivities, the components that have a large influence on the magnitude can be identified.

3. **Use Capacitance magnitude sensitivities to identify a capacitance that will improve $|S_{11}|$ and have minimal effect on the phase response.**
   Fig. 5.9 shows the result of T_d compensated S_{11}.



(a) Reflection coefficient magnitude. (b) Reflection coefficient phase.

Figure 5.9: T_1 $T_d = 185\ ps$ compensated results of limiter reflection coefficient magnitude and phase.

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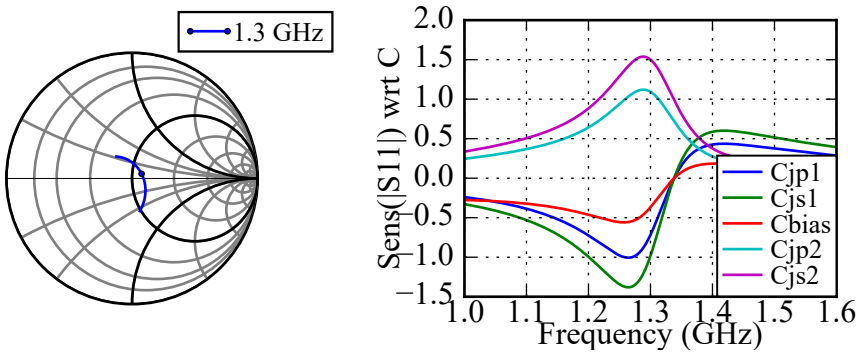
If the S_{11} magnitude sensitivities to variation in capacitor values in Fig. 5.10b are considered, it is seen that a variation in C_{js2} will result in the largest S_{11} magnitude variation.



(a) Reflection coefficient on Smith chart. (b) Sensitivity S_{11} magnitude with respect to variations in capacitor values.

Figure 5.10: T_1 $T_d = 185\ ps$ compensated results of limiter Smith chart and S_{11} magnitude sensitivity to capacitor variations.

For this example, S_{11} magnitude is improved at 1.3 GHz from $|0.05|$ to $|0.04|$. Taking Eq. 5.2.8, the required change in C_{js2} for a 0.01 decrease in reflection coefficient magnitude is calculated:

$$\Delta g_{k\_j} = \frac{\Delta |Y_{out}|\_j}{|Y_{out}|\_j} \frac{g_{k\_j}}{\mathrm{Re}\left(S_{g_{k\_j}}^{Y_{out\_j}}\right)} = 0.064\text{x}10^{-9} \tag{5.2.10}$$

To reduce $|S_{11}|$ by 0.01, C_{js2}'s value has to be decreased by $0.064\text{x}10^{-9}$ to $C_{js2} = 0.416\ pF$. Fig. 5.11 shows the improved S_{11} magnitude.

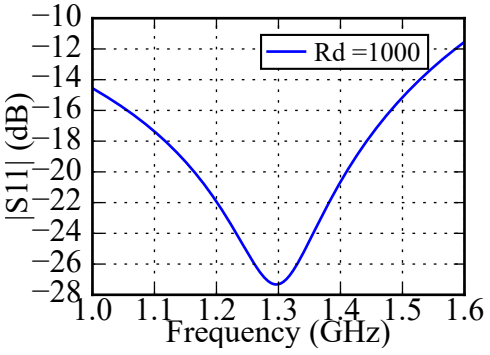


Figure 5.11: S_{11} of $T_d = 185\ ps$ and $C_{js2} = 0.416\ pF$ compensated limiter.

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4. **Repeat steps 1 - 3 to optimise S_{11} for a particular center frequency.**

It is important to remember that when variations are made with a particular phase sensitivity in mind, its corresponding magnitude variation should be consulted as well. This ensures that no unexpected changes in the input reflection coefficient's response occurs.

5.3 Simulation

Three sets of simulations are used to characterise the active PIN-Schottky limiter: small signal responses, large signal responses, and the 'coarse' PIN diode's thermal operation.

In this section, the limiter's small signal and large signal responses are given in different subsections. However, during the design, a change to improve small signal response should be followed by a large signal simulation. This ensures that an acceptable trade-off between good small signal parameters and large signal spike/flat leakage is found.

Once the limiter's small and large signal responses have been characterised, a thermal simulation is performed to ensure that the maximum allowable temperature of the limiter diode is not exceeded.

5.3.1 Small signal analysis

A small signal simulation is used to ensure a good reflection and transmission coefficient in the limiter's passing state.

The limiter in Fig. 5.12 is characterised with an *LTspice* simulation. The two Schottky diodes are included with *.model* commands given in Fig. 5.12. For the PIN diodes, the Caverly model is used, its *.lib* content is given in Appendix A.

The active PIN-Schottky limiter's S_{11}, S_{22} and S_{21} responses are shown in Figs. 5.13a and 5.13b.

In the design section, reflection coefficient improvement using sensitivity analysis was discussed. By varying the biasing transmission line's length and using it as a variable inductor, the effect of the large junction capacitance can be reduced and a more optimal reflection coefficient is found.

The results in Fig. 5.13a have already been optimised for reflection coefficient. The optimisation is limited by available component choice. By using the method described in Section 5.2.3 it is possible to find the best match for the available components.

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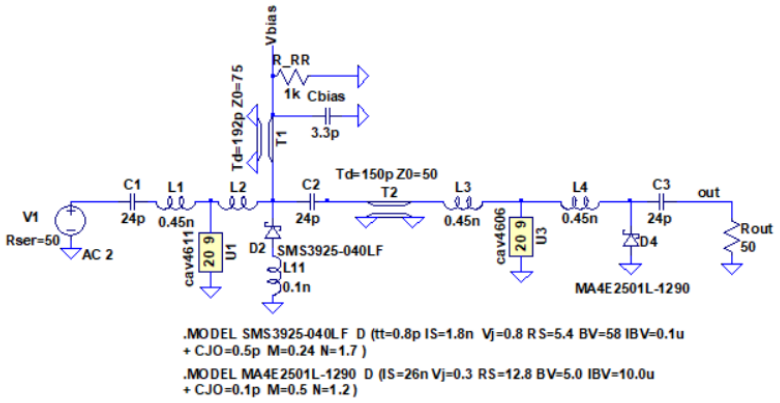
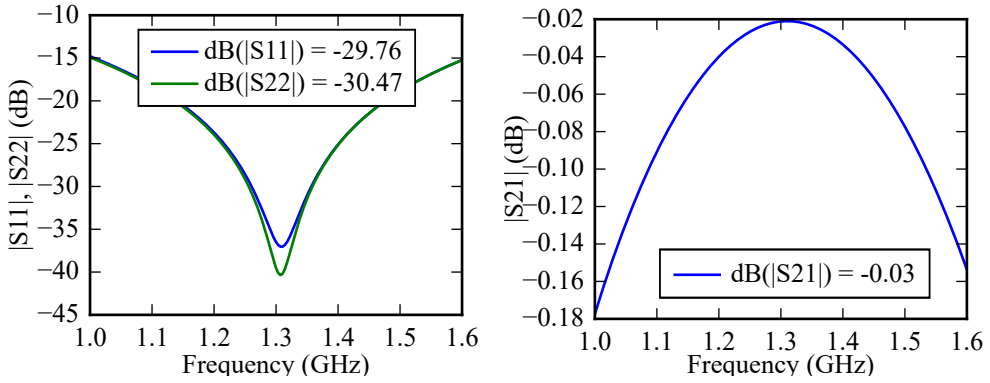


Figure 5.12: *LTspice* circuit diagram of the active PIN-Schottky limiter.



(a) Simulated reflection coefficient. (b) Simulated transmission coefficient.

Figure 5.13: *LTspice* simulation results of the active PIN-Schottky limiter.

5.3.2 Large signal analysis

Large signal analysis characterises the limiter's non-linear response to a large signal input. For pulsed operation, large signal analysis consists of the limiter's passive reaction to a large input signal as well as the limiter's subsequent passive recovery time.

The Caverly PIN diode model is used to simulate the limiter's active and passive large signal response in *LTspice*.

5.3.2.1 Active operation

The limiter's active operation protects sensitive components during the transmit cycle. For large signal measurements, an input power of 100 W peak with 16 % duty cycle is chosen. This is discussed further in the measurements section.

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For active operation simulation, a DC current of 200 mA is applied to the 'coarse' PIN diode and the subsequent output attenuation is given.

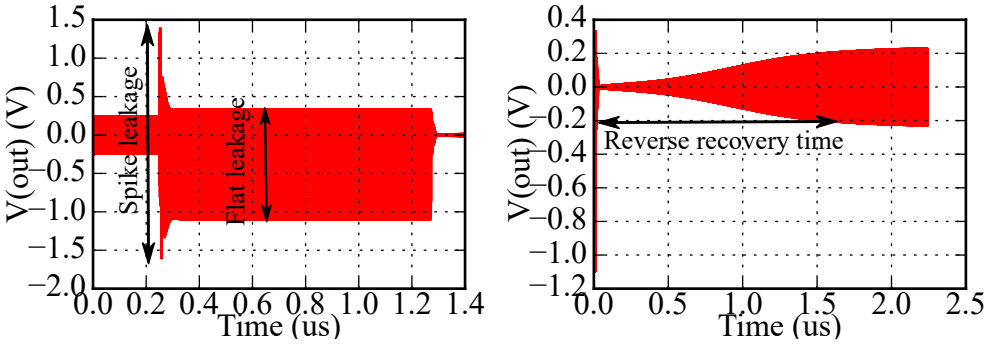
Active isolation is simulated to be more than 32 dB.

5.3.2.2 Passive operation set-up

In passive mode the limiter needs to handle a smaller input power than in active mode operation. An arbitrary passive peak power capability of approximately 3 W is chosen. The 3 W choice is explained in the measurements section. In a matched 50 Ω system, this translates to an input voltage of $\approx 35\ V_{pp}$.

5.3.2.3 Simulation results

The *LTspice* simulation of the passive limiter's spike leakage, flat leakage and reverse recovery time is given in Figs. 5.14a and 5.14b.



(a) Simulated spike and flat leakage

(b) Simulated reverse recovery time without R_{RR} in Fig. 5.12.

Figure 5.14: Simulated limiter spike and flat leakage, and reverse recovery time for a 35 V peak-to-peak input with 20 ns rise and fall time.

The limiter's simulated spike leakage in Fig. 5.14a is about 3 V_{pp}, which corresponds to a spike leakage power of $\approx$ 13 dBm. From Fig. 5.14a, the flat leakage is about 1.5 V_{pp} ($\approx$ 8 dBm).

In the simulation, a 20 ns rise time is used for the input pulse. The chosen rise time is determined by the rise time of the available power amplifier. A faster pulse rise time results in larger spike leakage in the limiter's response.

Fig. 5.14b shows the limiter's passive reverse recovery time. Reverse recovery time in passive operation is extremely slow ($\approx 1.6\ \mu s$), much longer than the 'coarse' PIN diode's minority carrier lifetime (300 ns). This is a problem that has been noted in available literature when using Schottky diodes instead of an RF choke to passively drive the PIN diode.

By using the resistor $R_{RR} = 1\ k\Omega$ as discussed in the design section, passive reverse recovery time can be improved significantly. The new reverse recovery

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time is given in Fig. 5.15 ($\approx 460\ ns$) and is clearly a big improvement to the reverse recovery time in Fig. 5.14b.

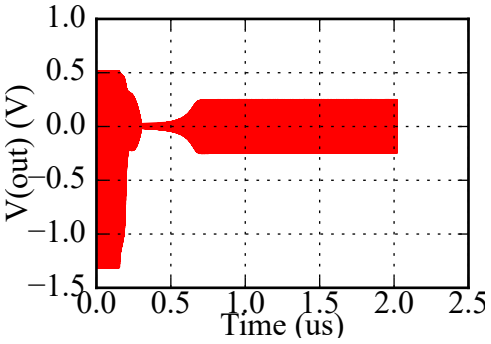

Figure 5.15: Improved passive reverse recovery time of active PIN-Schottky limiter.

5.3.3 Thermal analysis

A PIN diode's thermal response to power that is dissipated in the diode is modelled with a thermal simulation in *LTspice*. The diode's junction temperature increase is dependent on the heat removal path from junction to ambient.

Simulating the thermal response of a PIN diode in *LTspice* is a convenient solution that does not require expensive software.

In this section, the heat removal path from the PIN diode's junction to ambient is modelled using the thermal resistance and heat capacity of each element.

Fig. 5.16 shows a model of the heat path from the $CLA4611$'s I region to ambient. The main elements that are taken into account are: the diode, the copper strip that connects the diode to the vias, the vias, and the heat sink.

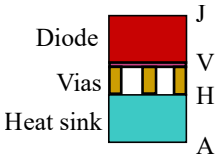

Figure 5.16: PIN limiter diode construction model. The diode is connected to the three vias through a copper strip, and the vias are connected to a heat sink via the copper ground plane of the PCB.

The ground pad of the *CLA4611* limits the size and number of vias that can be used; special consideration should be given to the vias' thermal resistance and heat capacity.

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The surface areas along which the heat travels in Fig. 5.16 is very small. This allows the assumption that heat is spread evenly on the surface where it is applied.

5.3.3.1 Thermal modelling

Consider the copper cube shown in Fig. 5.17.

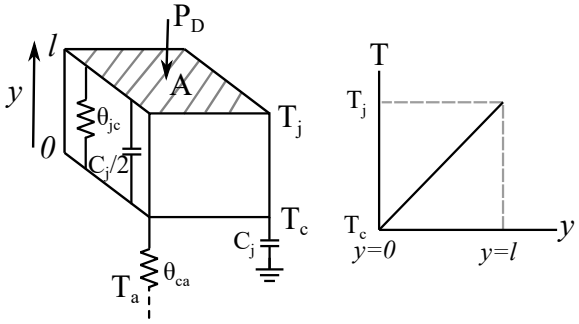

Figure 5.17: Copper cube. The graph shows the assumed linear temperature gradient of the cube. Assume a constant temperature distribution over the cube face's cross section (A).

If the temperature at the top face is T_j, the thermal resistance and heat capacity of the cube is modelled as shown in Fig. 5.18. C_j represents the heat capacity that is needed to raise the temperature of the cube from T_a to T_c. For a linear temperature gradient over the height (l) of the cube, $C_j/2$ is added in parallel with the thermal resistance θ_{jc}. $C_j/2$ represents the heat needed to raise the internal energy of the cube in order to increase the temperature of the upper face (at l) to T_j.

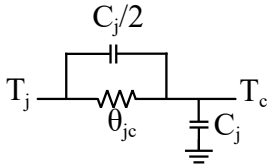

Figure 5.18: Thermal equivalent model of the cube of copper from Fig. 5.17.

The linear temperature gradient requirement is only met under stationary conditions. The thermal time constant is given by:

$$\tau_{jc} = \frac{l^2}{\alpha} \tag{5.3.1}$$

where α is the thermal diffusivity of the material.

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5.3.3.2 I and N layer thermal resistance and heat capacity

Consider the model of the PIN diode's I and N layers in Fig. 5.19 [2]. The radius of the I layer increases from its connection to the P layer up to its connection with the N layer. The N layer appears to take up most of the space in the PIN diode.

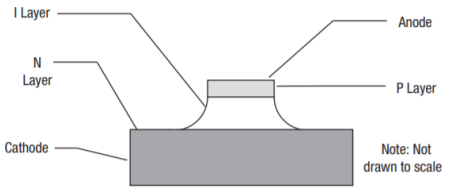

Figure 5.19: $CLA4611$ structure [2].

The dimensions of the *CLA4611* PIN diode's I and N layers are found in [56] and given in Fig. 5.20.

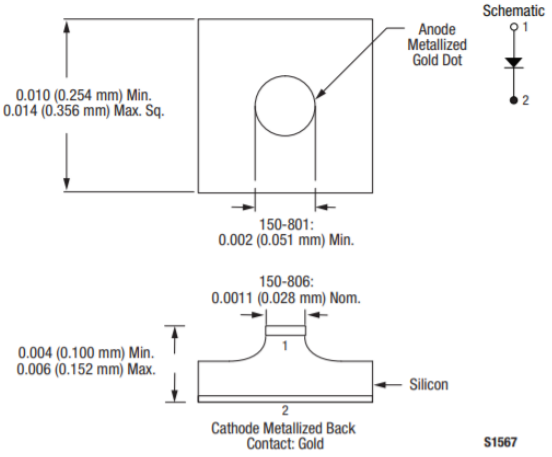

Figure 5.20: Dimensions of $CLA4611$'s P, I and N layer construction [56].

Due to the complex structure of the PIN diode, its thermal resistance and heat capacity are not easily calculated. The assumptions given in [2] are not sufficient for thermal analysis.

The $CLA4611$'s thermal resistance is given on its datasheet as 15 $^oC/W$. With this information, the measured thermal time constant can be used to calculate the PIN diode's heat capacity.

From Fig. 5.20, there is a big size difference between the diode's I and N layers, for this reason the two layers are modelled with separate thermal time constants. The I and N layer combined thermal model is given in Fig. 5.21.

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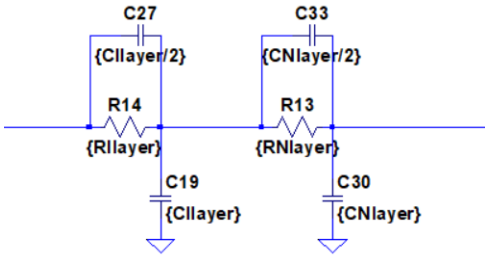

Figure 5.21: Distributed thermal model of PIN diode's I and N layers. The heat capacity added in parallel with the thermal resistances models the linear temperature gradient in that section.

The final thermal resistances and heat capacities of the PIN diode's I and N layers are derived from the measured junction temperature.

5.3.3.3 Via thermal resistance and heat capacity

The plating thickness of a via depends on the manufacturer, and can be as thin as 20 μm [52]. For a small via with a diameter of 0.2 mm, this value could be even smaller.

Consider a 0.508 mm thick PCB that has a copper cladding of 35 μm on both the top and bottom layer (total height: $h = 0.508 + 2\text{x}0.035\ mm$). If the vias have a diameter of 0.2 mm, and a plating thickness $t_{plating} \approx 15\ \mu m$ is assumed, the thermal resistance of a plated via is estimated as:

$$\theta_{via} = \frac{1}{\sigma}\frac{l}{A} = \frac{l}{\sigma\pi(r_o^2 - r_i^2)} \approx 172\ ^oC/W \tag{5.3.2}$$

where σ is the thermal conductivity of copper (385 W/Km [57]), l is the length of the via and A is the via's surface area with r_o the outer radius and r_i the inner radius of the plated via.

The thermal resistance of the plated via is surprisingly high.

Only three vias fit in the ground pad of the PIN diode, resulting in a total thermal resistance of $\approx 57.3\ ^oC/W$.

The heat capacity of a via with a diameter of 0.2 mm, a plating thickness of $\approx 15\ \mu m$, and height $h = 0.508 + 2\text{x}0.035\ mm$ is:

$$HC = \rho c_\theta V \approx 17.4\ \mu J/^oC \tag{5.3.3}$$

where ρ is the density of copper (8960 kg/m^3 [58]), c_θ is its specific heat (385 J/Kkg [59]) and V is its volume. The total heat capacity for three vias is $\approx 52.2\ \mu J/^oC$.

The thermal time constant of a single via is:

$$\tau_{via} = \theta_{via} HC_{via} \approx 2.992\ ms \tag{5.3.4}$$

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τ_{via} is much slower than the minimum expected pulse length of the applied signal (100 μs). The thermal model of the via has to be divided into multiple sections, where each section's thermal time constant is only a fraction of the minimum expected pulse length.

After multiple *LTspice* simulations, the thermal model of the vias starts to converge when 12 sections are used. Four sections of the model is shown in Fig. 5.22. An *LTspice* component is created from the four section model; the created component is used in cascade to create a twelve section model.

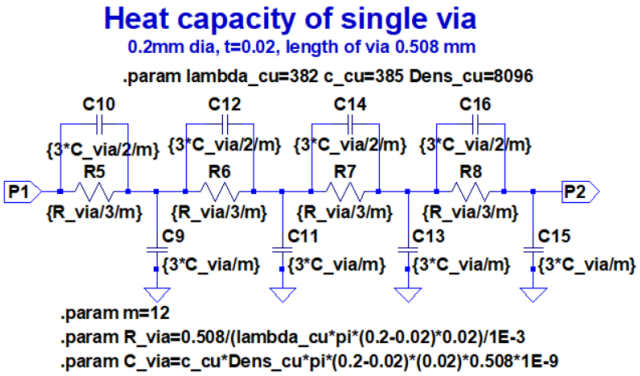

Figure 5.22: Distributed via model of three vias in parallel. A submodel consisting of four elements is shown, with a parameter $m = 12$. This submodel has to be repeated three times in the simulation to represent 12 sections.

5.3.3.4 Thermal model

The *LTspice* thermal simulation model of the PIN diode junction's heat removal path to ambient is given in Fig. 5.23.

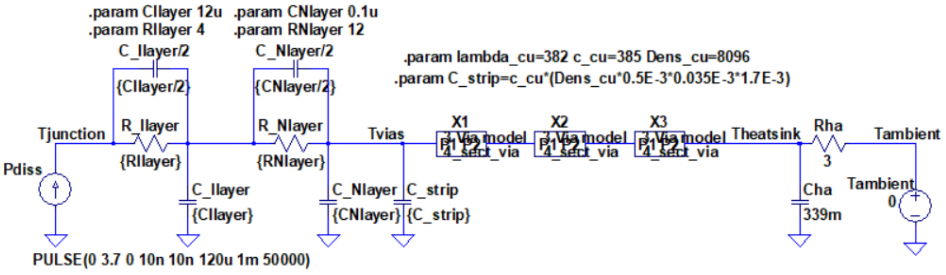

Figure 5.23: *LTspice* circuit analog of the construction shown in Fig. 5.16 [6].

Fig. 5.23 includes a thermal capacitance C_{strip} that is added by the copper strip where the PIN diode makes contact with the vias. The dimensions of the PIN diode's PCB footprint's ground pad is used to calculate C_{strip}.

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Using the equations given in Chapter 2, the heat capacities and thermal resistances of the different materials are calculated and given in Table 5.4.

Table 5.4: Calculated heat capacities and thermal resistances.

Parameter	Value	Units
C_{jc}	TBD	$\mu J/^oC$
R_{jc}	15	$^oC/W$
C_{strip}	92	$\mu J/^oC$
C_{vh}	17.4	$\mu J/^oC$
R_{vh}	172	$^oC/W$
C_{ha}	339	$mJ/^oC$
R_{ha}	3	$^oC/W$

The input to the simulation in Fig. 5.23 is a pulsed signal generated by a current source that represents the peak power dissipated in the PIN diode for each duty cycle.

The resistance of the PIN diode determines the power that is dissipated in the diode. However, the exact minimum attainable resistance for the *CLA4611* is not known. The minimum attainable resistance is achieved when the maximum allowable DC current is applied to the PIN diode (200 mA in this case).

A single resistance value at 10 mA is given on the *CLA4611*'s datasheet. This value is the sum of the N layer resistance, bond wire resistance and the the I layer resistance.

According to the *CLA4611*'s datasheet, the maximum CW power that can be dissipated in the diode is 2 W, and the maximum peak power that can be dissipated is 20 W at a 10 % duty cycle. The datasheet uses 1 μs pulses.

From the datasheet, the maximum DC current that can be applied to the *CLA4611* is 200 mA.

The ground pad of the *CLA4611* only fits three small vias. This severely limits the heat removal from the PIN diode's junction to ambient. For better heat removal, a smaller via thermal resistance is required. However, the only way to achieve a smaller thermal resistance is if the via diameter is larger, the via plating is thicker, the via is shorter or the via is filled with copper. Ideally, copper filled vias should be used. Currently, to the author's knowledge, there are only a few manufacturers that can copper fill vias.

Due to manufacturing restrictions, copper filled vias could not be used for the prototype.

5.4 Characterising measurements

The active PIN-Schottky limiter's small signal and passive large signal measurements are documented in this section.

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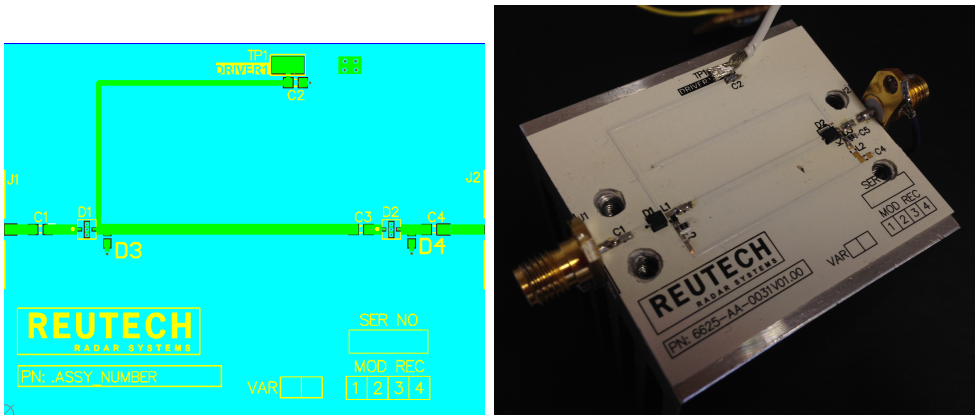
The limiter's small signal parameters are measured with a vector network analyser (VNA). In Section 5.4.1, the test set-up is given, followed by the results and a brief discussion of how the simulated and measured results compare.

In Section 5.4.2, the passive large signal test set-up is described. The limiter's passive operation is measured followed by a short comparison with the simulated data.

The PCB layout and manufactured limiter is given in Figs. 5.24a and 5.24b. The limiter was implemented on *RO4003C* 0.508 *mm* substrate. The input and output are connected through panel mount SMA connectors. The bottom layer of the PCB in Fig. 5.24b is exposed copper. Thermal paste is used on the bottom layer below the two PIN diodes to ensure good heat transfer from the vias to an aluminium heatsink.



(a) Limiter PCB layout. (b) Manufactured limiter

Figure 5.24: PCB layout of active PIN-Schottky limiter along with the manufactured circuit.

5.4.1 Small signal measurements

5.4.1.1 Test set-up

A VNA is used to measure the reverse biased limiter's small signal parameters. The set-up is shown in Fig. 5.25.

The VNA is calibrated over a frequency range 1 GHz to 1.6 GHz and an input power of -10 dBm is used. A small input power is used to ensure that the limiter is in its 'passing' state.

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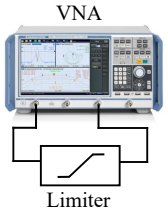
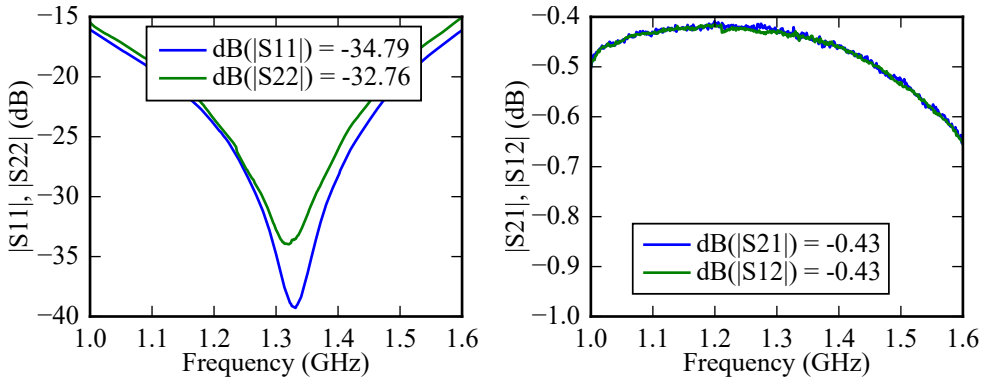


Figure 5.25: VNA set-up to measure limiter in its passing state.

5.4.1.2 Results

The limiter's reflection and transmission coefficients are shown in Fig. 5.26. The limiter has excellent small signal responses.



(a) Measured reflection coefficient (b) Measured transmission coefficient

Figure 5.26: Reflection and transmission coefficients of the limiter in its passing state.

If the measured small signal response is compared to the simulated response, there is good agreement between the two. In terms of the transmission coefficient, the loss is higher in the measured S_{21} since the *LTspice* simulation does not take microstrip loss into account.

5.4.2 Large signal passive measurements

The measurements in this section are used to confirm the active PIN-Schottky limiter's passive spike leakage, flat leakage, reaction time and reverse recovery time.

A digital oscilloscope (*DPO 7254* [60]) is used to measure the limiter's passive response. To characterise the limiter's passive operation, an input power of $\approx 6\ W$ peak is combined with a 355 mV_{pp} CW signal. After the combiner the input power that is incident on the limiter is $\approx 3\ W$.

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5.4.2.1 Test set-up

The measurement set-up used to characterise the limiter's passive operation is shown in Fig. 5.27. The high power amplifier (HPA) outputs a pulsed power

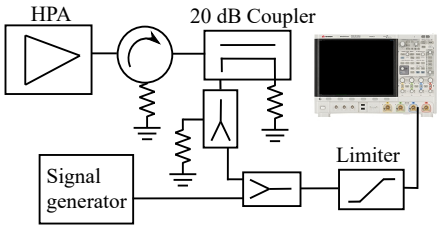

Figure 5.27: Test set-up to measure passive large signal response of limiter. A CW 355 mV_{pp} signal is combined with a $\approx 6\ W$ pulsed (10 % duty cycle) signal and measured on a digital oscilloscope.

of 1.3 kW (61.3 dBm) peak with a duty cycle that can be varied up to 16 %. A high power circulator is used to isolate the HPA from any limiter reflections. A 20 dB coupler lowers the peak power of the HPA to 41.3 dBm, and a 3 dB divider further lowers the peak power to 37.9 dBm. Finally, a 3 dB combiner is used to add the pulsed signal to a smaller CW signal.

The final signal that is applied to the limiter is pulsed with a peak power of approximately 3 W (35 V_{pp}). Combining the pulsed signal with a 355 mV_{pp} ($\approx -5\ dBm$) CW signal supplied by a signal generator allows the limiter's spike leakage and reverse recovery time to be measured.

The digital oscilloscope has a 2.5 GHz bandwidth that will filter harmonics from the limiter's output. When the measurements and simulation results are compared, this has to be taken into account.

5.4.2.2 Results

Fig. 5.28 shows the limiter's turn-on response to a large input pulse signal. The spike leakage seen in Fig. 5.28 is the initial power that passes through the PIN diodes before they turn on. The Schottky diodes ensure that the turn on transient of the limiter is faster than the case where an inductor is used.

The HPA switches on in 10 ns which is much faster than would be expected in a practical system (typically 100 ns). Due to the fast switching of the HPA, the spike leakage in Fig. 5.28 is much larger than would normally be the case.

The measured spike leakage in Fig. 5.28 is approximately 2.9 V_{pp}, which corresponds to a leakage power spike of just over 13 dBm. The fast switching time of the HPA significantly increases the spike leakage.

A flat leakage of about 1.2 V_{pp} (between 5 and 6 dBm) is measured. The passive limiter provides about 30 dB of isolation.

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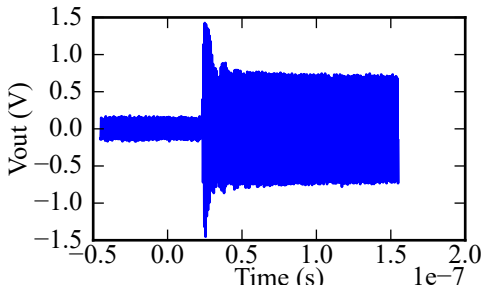
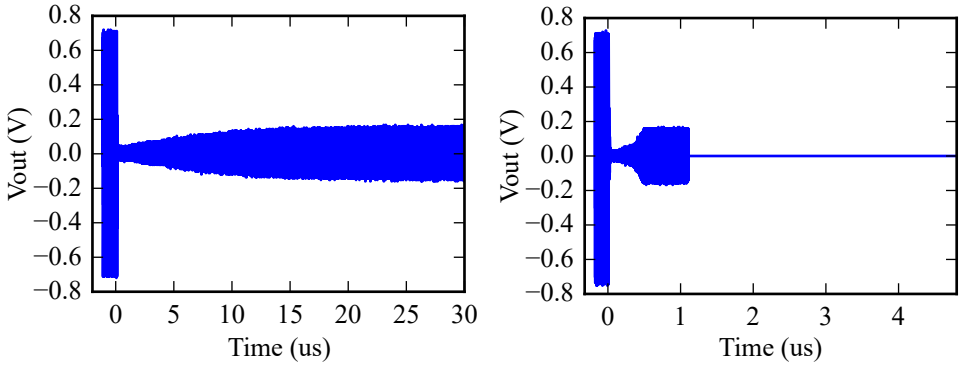


Figure 5.28: The limiter's spike and flat leakage for a 6 W input combined with a 316 mW CW input power.

Reverse recovery time is the time the limiter takes to recover to normal operation after a large signal was applied. This time is crucial for a radar, it determines how long the radar is prevented from reliably detecting targets again (once the limiter has stopped attenuating). The reverse recovery time is measured here when the CW signal has recovered to 80 % of its original value. The 80 % of the final value measure was chosen arbitrarily.

Fig. 5.29a shows the passive reverse recovery time of a limiter with an anti-parallel Schottky diode. Without an active driver removing excess charge carriers from the PIN diode, the reverse recovery time is much slower ($\approx 16\ \mu s$) than the PIN diode's minority carrier lifetime. The measured passive reverse recovery is even slower than the simulated reverse recovery time.



(a) No resistor, reverse recovery $\approx 16\mu s$. (b) 1 $k\Omega$, reverse recovery $\approx 350ns$.

Figure 5.29: The limiter's reverse recovery time for a 6 W pulsed and 316 mW CW combined input. By adding a resistor to ground at the end of the limiter's biasing line, the reverse recovery time is made significantly faster.

New improved reverse recovery time

Fig. 5.29b shows a much improved reverse recovery time compared to Fig. 5.29a. Through the addition of a single 1 $k\Omega$ resistor to ground at the end of the

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biasing line, the limiter's passive reverse recovery time can be improved significantly. The measured reverse recovery has been shortened to below 400 ns.

The addition of a resistor to improve reverse recovery time of a limiter with Schottky diodes is an improvement to passive limiter operation.

5.5 Thermal measurements

The 'coarse' PIN diode handles most of the input power during the limiter's blocking state.

Temperature increase in the PIN diode is related to the power that is dissipated in the diode as well as the subsequent thermal removal path from the diode's junction to ambient.

The PIN diode's resistance determines how much power the diode dissipates. Minimum attainable resistance is often not given by manufacturers, and the value is difficult to measure in the presence of series inductance. Estimating an active limiter's maximum input power handling capability is challenging.

The change in a PIN diode's junction temperature is related to its forward voltage by $\approx -2\ mV/^oC$ [61]. By monitoring the 'coarse' PIN diode's voltage decrease for a pulsed high power input, the diode's junction temperature is known for that particular set-up.

Section 5.5.1 measures the *CLA4611* PIN diode's junction temperature increase versus its diode voltage decrease for a specific forward bias current (200 mA).

Section 5.5.2 describes the tests and the respective test set-ups that are used to characterise the actively biased PIN diode's temperature response to high input power. By applying a large pulsed input signal while measuring the DC biased (200 mA) PIN diode voltage, the PIN diode's junction temperature increase is monitored.

Finally, the measured junction temperature curve is compared to the junction temperature increase of the thermal model that was created in Section 5.5.3. The simulated junction temperature is fitted to the measured junction temperature by adjusting the input peak dissipated power of the simulation. Through this comparison it is possible to estimate the minimum attainable resistance of the PIN diode.

5.5.1 Junction temperature vs. forward voltage calibration

In order to correctly measure and use the PIN diode's junction temperature dependence on forward voltage, the bias current has to be the same during temperature calibration and active limiter measurements.

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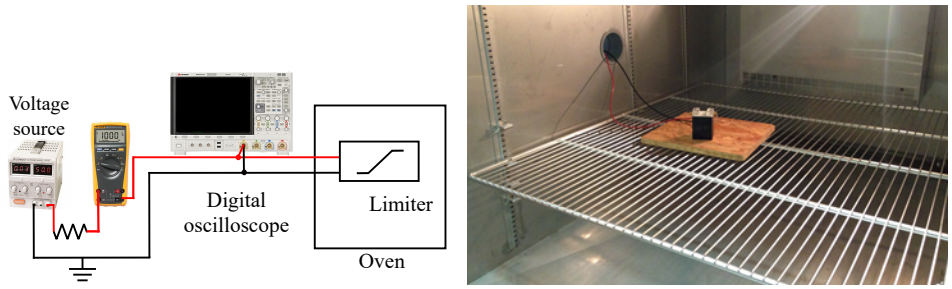
5.5.1.1 Measurement set-up

By placing the limiter in an oven and controlling the temperature around the PIN diode, junction temperature increase is emulated. Fig. 5.30 shows the test set-up to document the PIN diode's forward voltage versus junction temperature change.



(a) Measurement set-up. (b) Photo of set-up.

Figure 5.30: Junction temperature versus diode forward voltage calibration set-up. The PIN diode is forward biased with 200 mA during the measurement.

In Fig. 5.30, a voltage source is connected in series to a resistor, a multimeter, and to the limiter's biasing section. The resistor sets the current, and the multimeter is used to measure the current that is supplied to the limiter's 'coarse' PIN diode. During the oven measurements, the current applied to the PIN diode is continually monitored to ensure that the current remains the same.

The PIN diode is forward biased with the maximum allowable DC current(200 mA) to ensure the diode's equivalent I layer resistance is at its minimum value.

The voltage drop over the PIN diode is observed on the digital oscilloscope as the ambient temperature inside the oven is increased. A DC offset voltage is used on the oscilloscope to measure the diode voltage on a 5 mV per division scale. A sufficient time is allowed for the PIN diode to stabilise between temperature adjustments and forward voltage measurement readings.

Care was taken to ensure an accurate measurement.

5.5.1.2 Results

The diode voltage decrease for junction temperature increase is shown in Fig. 5.31.

The PIN diode's forward voltage decreases by about 1 $mV/^o\ C$. This is slightly lower than the values given in White [61] or Sickel [20].

With the relationship between the diode's forward voltage and junction temperature known, the power dissipated in the PIN diode during high power measurements can be monitored.

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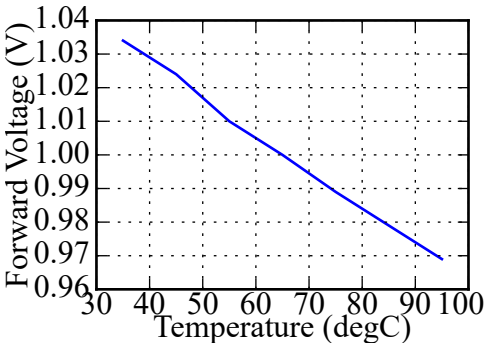

Figure 5.31: Measured actively biased PIN diode forward voltage versus junction temperature increase.

5.5.2 Measuring the PIN diode forward voltage for high input power

The maximum input power handling capability of a compact surface mount limiter is unknown when the PIN diode's minimum attainable resistance is unknown.

This section discusses a method of monitoring the PIN diode's junction temperature increase; the junction temperature increase is used in turn to find the PIN diode's minimum attainable resistance.

5.5.2.1 Test set-up

The set-up to measure the PIN diode's junction temperature change for a high power input signal is given in Fig. 5.32. The measurement set-up consists of a high power amplifier (HPA), a circulator, lossy cables and a power divider. The HPA outputs a pulsed signal; its duty cycle can be varied.

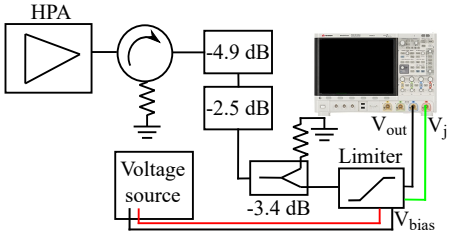

Figure 5.32: Measurement test set-up to determine the junction temperature of the PIN diode for a given input power.

The HPA outputs 61.4 dBm at a maximum 16 % duty cycle. Two long transmission lines are used to obtain losses of 4.9 dB and 2.5 dB respectively, resulting in a pulsed peak power of 54 dBm. Lastly, a power divider is used

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to reduce the peak power with a further 3.4 dB. The peak power used as the limiter's input is $\approx$ 50.5 dBm or $\approx$ 112 W when circulator loss is included.

An input signal with a 10 %, 12 %, 14 %, 16 % duty cycle and 112 W peak power is applied to the limiter. It was possible to obtain 112 W with the given HPA, couplers and dividers.

By monitoring the PIN diode's voltage, it is possible to see the junction's temperature increase for each pulsed input signal.

5.5.2.2 Results

Fig. 5.33 shows the PIN diode's forward voltage when the diode is DC biased with 200 mA and no RF signal is applied. From this measurement, the room temperature during the test is equated to a forward voltage of 1.045 V ('ambient' reference).

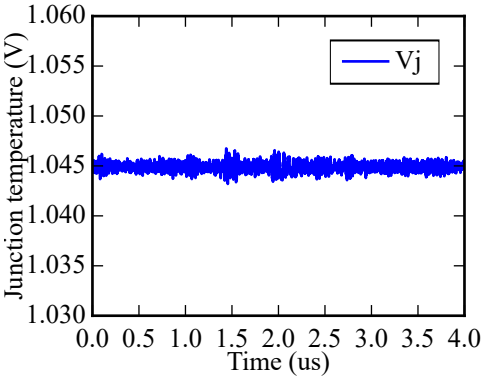

Figure 5.33: The PIN diode's forward voltage when it is forward biased with 200 mA and no RF signal is applied. This is referred to as the 'ambient' reference of the forward voltage. The 'ambient' reference is used as an equivalent to room temperature in the equations that follow.

To ensure safe operating conditions for the 'coarse' PIN diode, its maximum junction temperature of 175 ^oC should not be exceeded. If an ambient temperature of 20 ^oC is maintained, it follows that a diode voltage drop of 155 mV results in a junction temperature of 175 ^oC.

Measurement

For the measurement, the 'coarse' PIN diode is forward biased with 200 mA, and a pulsed 50.5 dBm RF signal is applied to the limiter.

The 'coarse' PIN diode's measured forward voltages for increasing duty cycles are given in Fig. 5.34. The 'on' time of the RF signal is seen in Fig. 5.34 as a decrease in diode voltage. The decrease in diode voltage translates to a junction temperature increase.

When the RF signal is turned on, there is an initial transient response where the thermal time constants of the vias and heat sink are visible. The

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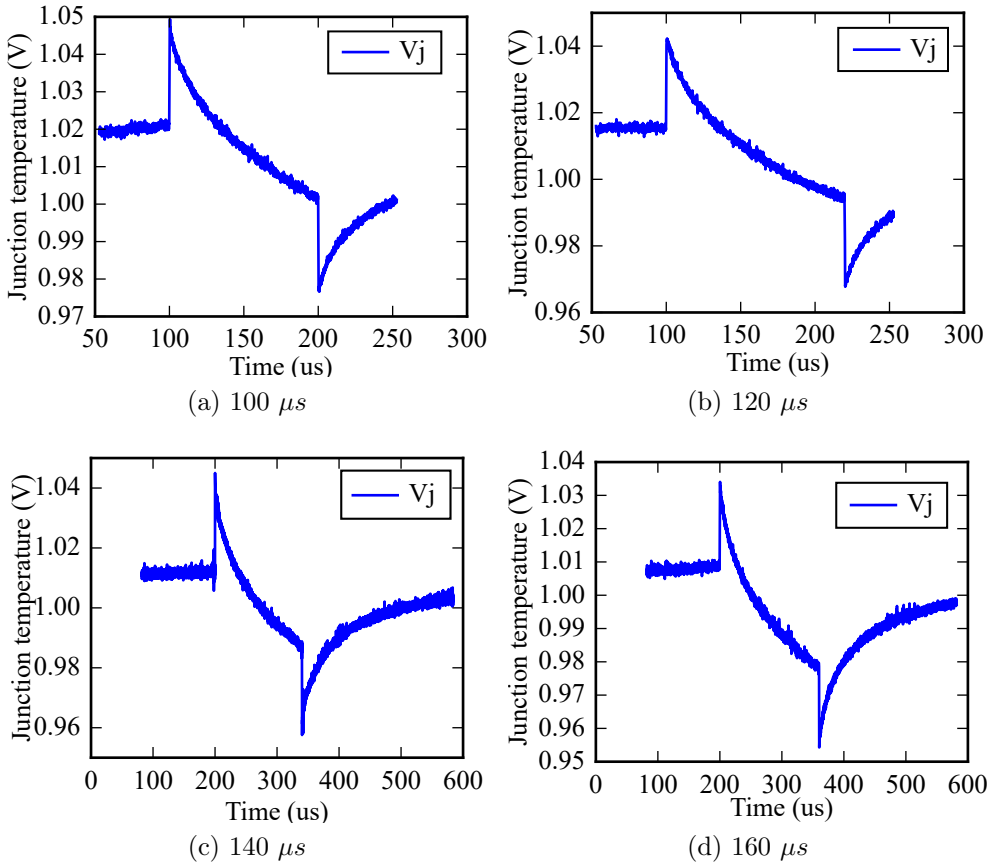

(a) 100 μs (b) 120 μs

(c) 140 μs (d) 160 μs

Figure 5.34: Forward voltage drop over 200 mA forward biased PIN diode for 112 W, 10 %, 12 %, 14 %, 16 % duty cycle input.

diode voltage measurements were taken after the voltage response had reached a steady state.

Discussion

At the leading edge of the measured diode voltages in Fig. 5.34, the diode's forward voltage suddenly increases and at the trailing edge it decreases. This behaviour is attributed to the large RF input signal that is converted to a DC current through a non-linear mechanism of the diode. The increased bias current in turn increases the forward voltage. Once the pulse ends, the additional biasing current ends and the forward voltage returns to its expected level. These jumps in forward voltage do not have any effect on the temperature measurements.

If we refer back to Fig. 5.33, the diode voltage at 'ambient' (no RF signal present) is measured as 1.045 V. From Fig. 5.34, the average diode forward voltage decreases with $(1.045 - 1.02 = 20\ mV)$ which means the temperature increases by 20 ^oC above ambient (kept at 20 ^oC), with its peak temperature reaching $(1.045 - 0.985 = 60\ mV)$ 60 ^oC above ambient.

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When the pulse length is 160 μs, the average temperature of the PIN diode's junction has increased by 30 ^oC above ambient with peak increase of 80 ^oC above ambient.

5.5.3 Extracting a thermal model

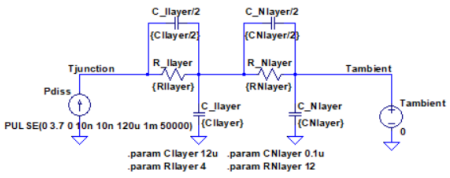
The input to the thermal simulation is the power that is dissipated in the PIN diode. By changing P_{diss} in the simulation, the thermal model's response is adjusted until a good fit is found to the junction temperature measurements.

When a high power RF signal is applied to the forward biased PIN diode, the diode voltage changes from the 'ambient' reference with each input pulse. The PIN diode's thermal time constant is fast and can be expected to nearly reach its final value in the on-time of the pulse (100 μs – 160 μs).

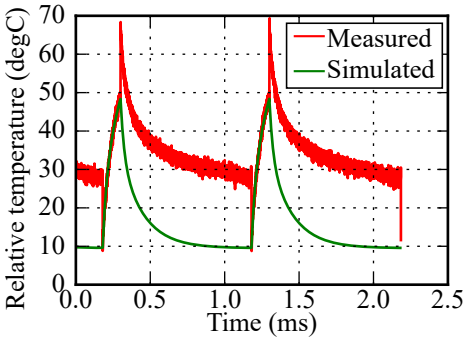
5.5.3.1 PIN diode thermal time constant

The PIN diode's thermal time constant is found by comparing the measured diode voltage response to the diode's thermal model response in *LTspice*. Two thermal time constants are used to model the I and N layers.

LTspice is used to plot the measured junction temperature against the diode's simulated junction temperature. Fig. 5.35 shows the result of the fitted I and N layer thermal time constants.



(a) *LTspice* I and N layer thermal model.



(b) Fitted result.

Figure 5.35: Fitted thermal models of the I and N layers. The total thermal resistance is still within the thermal resistance value range that was given on the $CLA4611$'s datasheet.

The apparent decrease and increase of temperature at the start and end of each pulse in Fig. 5.35 is the result of current rectification due to a non-linear operation of the PIN diode when a large RF signal is applied. Both the 'on' and 'off' time curve of the simulated junction temperature fits on the measured junction temperature.

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5.5.3.2 Complete thermal model

The vias connecting the PIN diode's ground paddle to the heat sink has a slow time constant compared to the applied pulse's on-time. The heat sink also has a slow thermal time constant. The calculated and fitted thermal resistances and heat capacities are repeated in Table 5.5.

Table 5.5: Calculated and fitted heat capacities and thermal resistances of the PIN diode and its thermal path to ambient.

Parameter	Value	Units
C_{ILayer}	12	$\mu J/^oC$
R_{ILayer}	4	$^oC/W$
C_{NLayer}	0.1	$\mu J/^oC$
R_{NLayer}	12	$^oC/W$
C_{vh}	17.4	$\mu J/^oC$
R_{vh}	172	$^oC/W$
C_{ha}	339	$mJ/^oC$
R_{ha}	3	$^oC/W$

Fig. 5.36 gives the complete *LTspice* model that simulates the 'coarse' PIN diode's thermal response to power that is dissipated in the diode.

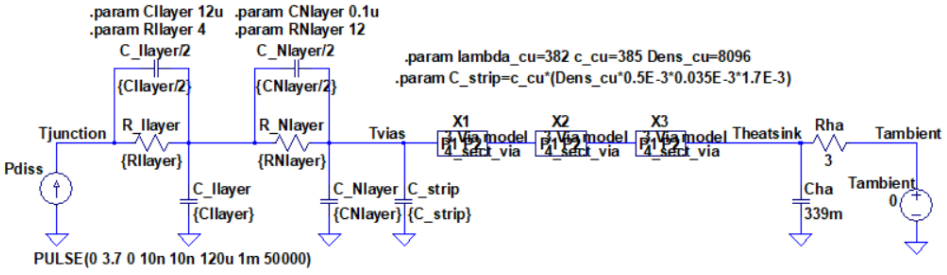

Figure 5.36: *LTspice* diagram of thermal model. The ambient temperature was set to 0. This made it easier to compare the simulated and measured junction temperature.

The measured and simulated junction temperature is plotted in Fig. 5.37, normalised to ambient temperature. Both the measured and simulated data is taken after the initial temperature transient has settled. The slow transients are due to the slower thermal time constants of the vias and heat sink in the circuit.

Fig. 5.37 shows the best fit between the simulated and measured junction temperatures. The best fit is found where a peak power of 3.7 W is dissipated in the PIN diode.

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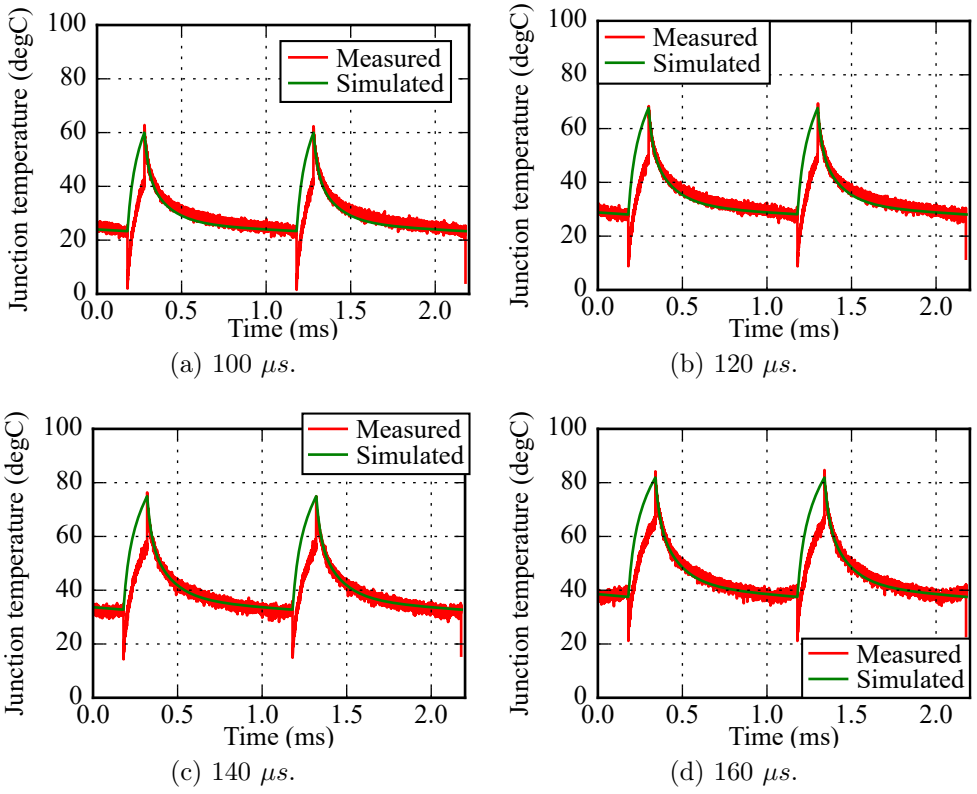

(a) 100 μs. (b) 120 μs.

(c) 140 μs. (d) 160 μs.

Figure 5.37: Comparison of thermal model to measured diode voltage response for pulsed input power. The 'ambient' reference was set to 0 to compare the simulated and measured results better.

5.5.3.3 Extracted dissipated power and minimum resistance

By fitting the measured junction temperature to simulated junction temperature, the peak power that is dissipated in the 'coarse' PIN diode is found. For $P_{in} = 112\ W$, $P_d = 3.7\ W$ and $Z_0 = 50\ \Omega$, the PIN diode's minimum attainable resistance is calculated as:

$$(R_s + R_d) = P_d \frac{Z_0}{4P_{in}} = 0.412\ \Omega \tag{5.5.1}$$

The calculated minimum resistance is much larger than initially assumed.

5.5.3.4 Confirm extracted values

Testing the extracted minimum resistance, a 12 W peak input power with a 10 % duty cycle is used.

Calculating the peak power dissipated in the PIN diode:

$$P_d = \frac{4P_{in}(R_s + R_d)}{Z_0} = \frac{4\text{x}12\text{x}0.412}{50} = 0.39\ W \tag{5.5.2}$$

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The resulting simulation and measurement for a 12 W peak input power is shown in Fig. 5.38. The measured and simulated results are in good agreement.

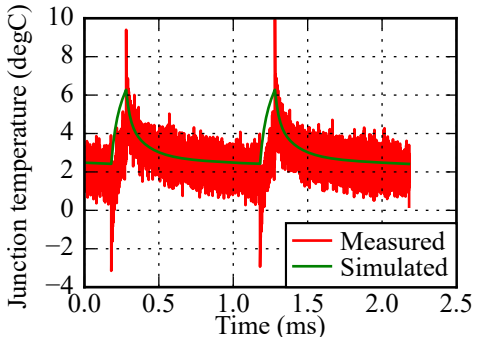

Figure 5.38: Confirming the extracted minimum resistance by comparing thermal simulation and measurement for a 12 W peak input power.

5.5.3.5 Extracting minimum attainable resistance through S-parameters

Using S-parameters, it is possible to approximate the PIN diode's minimum attainable resistance and compare it to the resistance value extracted through the high power measurement method.

By plotting the limiter's measured transmission coefficient for a bias current of 200 mA, the series inductance can be estimated. Consider the transmission coefficient magnitude in Fig. 5.39. When the series inductance dominates the limiter's reflection coefficient, the transmission coefficient will have a positive slope of 20 dB per decade. Once this slope is identified, the inductance value is calculated from the equivalent impedance at a particular frequency. From

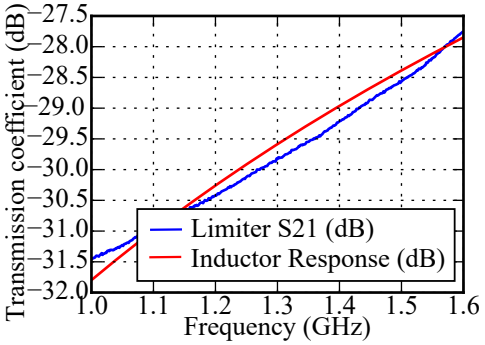

Figure 5.39: Limiter's measured transmission coefficient for forward bias current equal to 200 mA.

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Fig. 5.39, the series inductance is calculated as approximately 0.105 nH.

Using a simplified small signal model of the limiter in *LTspice*, the measured change in transmission coefficient is compared to the simulated transmission coefficient. The PIN diode's resistance is varied until the best fit is found. The best fit of the PIN diode's resistance is found to be 0.41 Ω. This value is similar to the minimum attainable resistance extracted through the high power measurement method.

5.6 Conclusion

A compact high power active PIN-Schottky limiter was developed in this chapter.

Circuit layout and component options were discussed first. A novel application of sensitivity analysis was described. It was shown that sensitivity results could be used to identify critical components that affect the reflection coefficient, and to use those components to optimise the reflection coefficient at a particular frequency.

An *LTspice* simulation was performed for both small signal and large signal behaviour. The small signal parameters (transmission and reflection coefficients) were simulated, and with the use of sensitivity results as discussed in the previous section, the reflection coefficient was optimised for a particular center frequency. Using the Caverly PIN diode model in *LTspice*, the large signal response of the limiter was simulated. Finally, *LTspice* was used to simulate the PIN diode's junction temperature increase for a pulsed input power.

The first set of measurements in Section 5.4 gave the limiter's small signal and passive large signal operation. In this Section an improvement to passive limiter recovery was proposed. Through the addition of a single resistor the limiter's passive reverse recovery time was shortened significantly.

It is impossible to estimate the PIN diode's minimum attainable resistance from datasheet parameters when a resistance at a single forward current is given. It is also difficult to reliably measure the PIN diode's minimum resistance on a VNA due to diode and package series inductance dominating the response at high frequencies. The resistance determines how much power is dissipated in a diode, which in turn limits the maximum input power.

In Section 5.5, a temperature calibration was performed on the 'coarse' PIN diode to find its forward voltage relation to junction temperature. The limiter was placed in an oven, and the PIN diode's voltage for a bias current of 200 mA was measured as the temperature was increased. It was found that the diode voltage decreased by 1 $mV/^oC$. Next, the PIN diode's junction temperature increase could be monitored for a large pulsed input power.

By fitting the junction temperature increase to a thermal model of the PIN diode's junction to ambient heat removal path, it was possible to estimate the

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PIN diode's minimum attainable resistance.

1. The limiter's reflection coefficient was optimised through the application of sensitivity analysis.
2. The PIN-Schottky passive limiter's reverse recovery time was improved significantly.
3. High power measurements were used to determine the minimum attainable resistance of a PIN diode in a high power limiter.

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Chapter 6

Conclusions

Multi-channel DBF radar uses the measured phase difference between its receiver channels to determine the direction of arrival of target returns. Accurate relative phase measurement between channels will result in a better DoA estimation. EVAs are used before the receivers' LNAs for STC to prevent receiver saturation. These EVAs need to track in phase and have minimal insertion loss. Additionally, the receivers need to be protected from large signals that damage sensitive components. Three distinct topics were covered in this dissertation:

1. An RSS phase error measure was derived in Chapter 3. This RSS phase error measure showed the expected RMS phase error of an electronic network due to component tolerances.
2. An optimal phase tracking set of EVAs was developed in Chapter 4.
3. A compact high power limiter was designed. The limiter's power handling capability was characterised through high power measurements discussed in Chapter 5.

6.1 Sensitivity analysis

Sensitivity analysis was used to find the relative output phase sensitivity of a network due to component tolerances.

To include a network's output sensitivity to transmission line dimensional tolerances, existing sensitivity equations had to be extended.

A method had to be devised to rank networks in terms of output phase variation due to component tolerances.

Contribution 1: Extend existing sensitivity analysis of lumped networks to create a generalised framework that accommodates both lumped and distributed elements. Use the sensitivity results to improve circuit performance.

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Chapter 3 discussed sensitivity analysis of lumped and distributed networks. A tool was created with which sensitivity analysis of lumped and distributed networks could be performed. The sensitivity analysis method discussed in Chapter 3 used a mathematical approach to solving a network's output sensitivities. The mathematical approach eliminated the need to construct the traditional adjoint network.

The sensitivity results were uniquely used to identify small component variations that could improve a particular network's performance, as shown in Chapter 4 and Chapter 5.

In Chapter 4, the parallel quarter-wave -and series quarter-wave attenuators' individual output and input phase sensitivities were considered. Through the interpretation of individual component sensitivities, it was found that both structures could be cascaded back-to-back to improve the output phase sensitivity and output reflection coefficient of each network.

In Chapter 5 the limiter's reflection coefficient sensitivity to lumped and distributed element variations was calculated. The reflection coefficient sensitivity results allowed the identification of specific components that could be varied to optimise the input reflection coefficient at a particular center frequency.

Contribution 2: Define an effective sensitivity error measure from the sensitivity results, suitable to rank the phase tracking performance of multiple electronic networks.
When applying sensitivity analysis to a network, multiple output sensitivities to component variations were found. It is difficult to usefully interpret the multiple output sensitivities of a given network. To find an estimate of the effect of component tolerances on the output phase of a set of networks, an error measure was defined in Chapter 3.

By taking the square root of the sum of the squared output variations, a single error measure was defined to give the expected RMS magnitude and phase error. The tolerances of lumped element values were assumed to be uncorrelated. The distributed elements have dimensional tolerances that affect the transmission line's characteristic impedance and propagation delay. Due regard was given to correlated and uncorrelated sensitivities.

A root sum square magnitude and phase error measure was developed in Chapter 3.

6.2 Electronically variable attenuators

An optimal phase tracking set of EVAs had to be identified. Using the RSS phase error measure defined in Chapter 3, several EVAs' phase tracking could be ranked over control range.

Contribution 3: Use the defined error measure to critically examine and compare the phase tracking performance of several PIN

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diode EVAs to identify an optimal phase tracking topology.
By comparing the RSS phase error of six matched electronically variable attenuator topologies, the CPQA was identified as having optimal phase tracking within a set of CPQAs.

Through the application of the RSS phase error measure, it was found that the output RSS phase error of a parallel quarter-wave attenuator could be improved by cascading the topology in a back-to-back configuration (CPQA).

In Chapter 4, a biasing scheme was proposed for the CPQA. Sensitivity analysis was applied to the CPQA with its biasing structure, identifying components that could be changed to improve the output RSS phase error. This novel approach to biasing structure analysis resulted in improved RF/DC isolation, attenuation flatness and reflection coefficient performance.

6.3 Compact high power limiter

Available literature provides methods to determine the power that is dissipated in a PIN diode given a set of parameters. There are methods to calculate how much the PIN diode's junction temperature increases when the dissipated power is known. Equations are also available to calculate the resistance of a PIN diode's I layer given the forward current. However, if a PIN diode's minimum resistance is unknown, the maximum power that can be dissipated in the PIN diode can not be determined reliably. The minimum resistance is limited by the physical resistance of the P and N layers as well as bond wire resistance.

A method was needed to determine the minimum attainable resistance of a PIN diode.

Using a Schottky diode instead of an inductor in anti-parallel with a PIN diode increased the limiter's reverse recovery time considerably. An improvement to PIN diode limiter operation was proposed.

Contribution 4: Develop an approach using high power measurements to characterise a high power limiter.
In Chapter 5, a high power measurement method was used to identify a PIN diode's minimum attainable resistance.

By measuring the PIN diode's voltage decrease for junction temperature increase, a junction temperature calibration term was identified.

The temperature calibration measurement was discussed in Chapter 5. The limiter was placed in an oven and its input diode voltage was monitored as the oven's temperature was increased. During the measurement, the limiter's 'coarse' PIN diode was forward biased. This ensured that the diode voltage 'ambient' reference was the same during the temperature calibration and the subsequent high power measurements.

A thermal model of the PIN diode's junction to ambient path was created in *LTspice* and used to compare the simulated temperature increase to the

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measured junction temperature increase. The power dissipated in the PIN diode's junction was adjusted in the simulation until the measured and simulated data fit. Once the dissipated power was known, it was possible to calculate the minimum attainable resistance of the PIN diode.

Contribution 5: Improving the passive PIN-Schottky diode limiter's reverse recovery time.
In Chapter 5, a resistor was added in parallel with the 'coarse' PIN diode's biasing line's decoupling capacitor. The addition of the resistor significantly improved the limiter's passive reverse recovery time.

Simulation and measurements confirmed that the reverse recovery resistor dramatically improved the passive limiter's reverse recovery time.

6.4 Final remarks

The three topics covered in this dissertation produced very useful results.

The RSS phase error measure allowed the identification of an optimal phase tracking set of EVAs. The optimal phase tracking performance of a set of CPQA was confirmed through measurements. The CPQA was also developed to have minimal insertion loss, a large attenuation range and a simple biasing scheme. All these attributes make the CPQA an excellent choice for use in a multi-channel digital beamforming receiver.

It was crucial to know the minimum resistance of the active PIN-Schottky limiter's 'coarse' PIN diode in order to know how much input power the limiter could handle. The power handling of the active PIN-Schottky limiter was characterised through the extraction of its minimum attainable resistance. The extracted results were confirmed through further high power measurements. An effective and compact high power limiter was developed.

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Appendices

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Appendix A

Caverly PIN diode model

```
*Caverley et al
*2000

.subckt cav4611 9 20 params: is=1e-10,
+ n=1, ikf=3, phi=.7, ie=6, iknee=.01
+ rlim=1.8m, repi=800k, cj=0.25p,
+ tau=300n, w=12u, lbond=0.06n, cpack=0.01p
+ b=3
.param to={w*w/.001935/4}
.param vm={w*w/tau/0.1}
.param alfa={to/tau}
.param npi={2*n/(1+b)}
.param nin={2*b*n/(1+b)}
cpack 9 20 {cpack}
lbond 9 10 {lbond}
cjunc 10 20 {cj}
repi 10 12 {repi}
rlim 10 11 {rlim}
grmod 11 12 value={2*(v(11,12)*v(2,3)/vm)}
gpin 12 20 value={i(vs2)}
rpin 10 20 1e12
ej 30 0 value={v(12,20)}
vs1 30 31 0
* two different junction models
dpi 31 32 dj1
din 32 0 dj2
.model dj1 d (is={is},ikf={ikf},n={npi})
.model dj2 d (is={is},ikf={ikf},n={nin})
e1 1 0 value={i(vs1)}
vs2 1 2 0
* ge describes the current-dependent tau
```

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```
ge 2 0 value={(v(2)*v(2))/iknee}
* 8th order approximation for base region
rp1 2 3 1
cp1 2 3 {tau}
rs1 3 0 {alfa/3}
rp2 3 4 5
cp2 3 4 {tau/5}
rs3 4 0 {alfa/7}
rp4 4 5 9
cp4 4 5 {tau/9}
rs5 5 0 {alfa/11}
rp6 5 6 13
cp6 5 6 {tau/13}
rs6 6 0 {alfa/15}
rp7 6 7 17
cp7 6 7 {tau/17}
rs7 7 0 {alfa/19}
.ends
```

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Appendix B

Sensitivity analysis

B.1 Netlist circuit analysis

B.1.1 Response and sensitivity

B.1.2 Setup

```
%matplotlib inline

from __future__ import division
import matplotlib.style
import matplotlib as mpl
mpl.style.use('classic')
import matplotlib
matplotlib.rcParams['font.family'] = 'Times New Roman'
matplotlib.rcParams['font.size'] = 12
matplotlib.rcParams['svg.fonttype'] = 'none'
from math import *
import numpy as np
import os
import matplotlib.pyplot as plt
import skrf as rf
plt.rc('legend',fontsize=10)
plt.rc('text', usetex=False)
```

B.1.3 Read netlist file (.txt)

```
f = open("lastfile.sna", "r")
fnl = f.readline()
f.close()

print(fnl)
```

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```
fileName = fnl + ".sna"
print "fileName plus extension:", fileName
print(fileName)
f = open("Circuit netlists/"+fileName, 'r')
newLine = True
for line in f:
    if newLine:
        l = [line]
        newLine = False
    else:
        l.append(line)
f.close()

f=open("lastfile.sna", "w")
print >>f, fnl,
f.close()
```

```
QuasiActiveLimiter
fileName plus extension: QuasiActiveLimiter.sna
QuasiActiveLimiter.sna
```

B.1.4 Parse the netlist

Extract element information into lists of elements and their attributes

```
def extractParams(l,Rd):
    comments = 0
    branches = 0
    nodes = 0
    R=[]
    C=[]
    L=[]
    T=[]
    G=[]
    er=[]
    #Number the branches in order resistors, capacitors, inductors,
    # transmission lines, VCCS
    for line in range(len(l)):
        if l[line][0]=="f":
            fr=l[line].split()
            frange= np.linspace(float(fr[1]),float(fr[2]),
                                int(fr[3]),True)
            findex = np.arange(int(fr[3]))
        if l[line][0]=="R":
            branches= branches+1
            tl=l[line].split()
```

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```
            if tl[0][1] == "d":
                R.append([branches, int(tl[1]),int(tl[2])
                            ,Rd,tl[0]])
            else:
                R.append([branches, int(tl[1]),int(tl[2])
                            ,float(tl[3]),tl[0]])
            nodes = np.max((nodes,int(tl[1]),int(tl[2])))
    for line in range(len(l)):
        if l[line][0]=="C":
            branches= branches+1
            tl=l[line].split()
            C.append([branches, int(tl[1]),int(tl[2]),
                      float(tl[3]),tl[0]])
            nodes = np.max((nodes,int(tl[1]),int(tl[2])))
    for line in range(len(l)):
        if l[line][0]=="L":
            branches= branches+1
            tl=l[line].split()
            L.append([branches, int(tl[1]),int(tl[2]),
                      float(tl[3]),tl[0]])
            nodes = np.max((nodes,int(tl[1]),int(tl[2])))
    for line in range(len(l)):
        if l[line][0]=="T":
            branches= branches+2
            tl=l[line].split()
            T.append([branches-1, branches, int(tl[1]),
                      int(tl[2]),int(tl[3]),
                      int(tl[4]),float(tl[5]),float(tl[6])
                          ,tl[0]])
            nodes = np.max((nodes,int(tl[1]),int(tl[2]),
                            int(tl[3]),int(tl[4])))

    for line in range(len(l)):
        if l[line][0]=="G":
            branches= branches+2
            tl=l[line].split()
            G.append([branches-1, branches, int(tl[1]),int(tl[2])
                          ,int(tl[3]),
                      int(tl[4]),float(tl[5]),tl[0]])
            nodes = np.max((nodes,int(tl[1]),int(tl[2]),int(tl[3])
                            ,int(tl[4])))
    for line in range(len(l)):
        if l[line][0]=="!":
            comments = comments+1
```

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```
        if l[line][0]=="I":
            tl = l[line].split()
            input_node = tl[1]
        if l[line][0]=="O":
            tl = l[line].split()
            output_nodes = [int(tl[1]),int(tl[2])]
    return comments, nodes, branches, R, C, L, T, G, findex, \
        frange, output_nodes, input_node
```

B.1.5 Summary of circuit and component attributes

Components lists formats

R,C,L: [branch, node 1; node 2; value; designator]

T: [branch (port 1); branch (port 2); port 1 node 1; port 1 node 2; port 2 node 1; port 2 node 2; Z_0; $T_d $; designator]

G: [branch (port 1); branch (port 2); port 1 node 1; port 1 node 2; port 2 node 1; port 2 node 2; $; g_m $; designator]

B.1.6 Setup the incidence matrix

```
def setupIncidenceMatrix(R,C,L,T,G,nodes,branches):
    A=np.zeros((nodes,branches),int)
    for r in range(len(R)):
        if R[r][1]<> 0:
            A[R[r][1]-1,R[r][0]-1]=1
        if R[r][2]<> 0:
            A[R[r][2]-1,R[r][0]-1]=-1
    for r in range(len(C)):
        if C[r][1]<> 0:
            A[C[r][1]-1,C[r][0]-1]=1
        if C[r][2]<> 0:
            A[C[r][2]-1,C[r][0]-1]=-1
    for r in range(len(L)):
        if L[r][1]<> 0:
            A[L[r][1]-1,L[r][0]-1]=1
        if L[r][2]<> 0:
            A[L[r][2]-1,L[r][0]-1]=-1
    for r in range(len(T)):
        if T[r][2]<>0:
            A[T[r][2]-1,T[r][0]-1]=1
        if T[r][3]<>0:
            A[T[r][3]-1,T[r][0]-1]=-1
        if T[r][4]<>0:
```

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```
            A[T[r][4]-1,T[r][1]-1]=1
        if T[r][5]<>0:
            A[T[r][5]-1,T[r][1]-1]=-1
    for r in range(len(G)):
        if G[r][2]<>0:
            A[G[r][2]-1,G[r][0]-1]=1
        if G[r][3]<>0:
            A[G[r][3]-1,G[r][0]-1]=-1
        if G[r][4]<>0:
            A[G[r][4]-1,G[r][1]-1]=1
        if G[r][5]<>0:
            A[G[r][5]-1,G[r][1]-1]=-1
    return A
```

B.1.7 Branch admittance matrices for R, C and L elements

```
def admittanceMatrices(branches,R,C,L):
    Rmat=np.zeros((branches,branches),float)
    Cmat=np.zeros((branches,branches),float)
    Lmat=np.zeros((branches,branches),float)
    Tmat=np.zeros((branches,branches),complex)
    for r in range(len(R)):
        Rmat[R[r][0]-1,R[r][0]-1]=1.0/R[r][3]
    #print "Rmat", Rmat
    for r in range(len(C)):
        Cmat[C[r][0]-1,C[r][0]-1]=C[r][3]
    #print "Cmat", Cmat
    for r in range(len(L)):
        Lmat[L[r][0]-1,L[r][0]-1]=1.0/L[r][3]
    #print "Lmat", Lmat
    return Rmat,Cmat,Lmat,Tmat
```

B.1.8 Branch admittance matrix for VCCS

B.1.9 Transmission line functions

Lines are described by $Z_0,;f,;T_d$

Admittance functions:

$$Y_i = \qquad y_{11} = y_{22} = \frac{-j}{Z_0 \tan(2\pi f T_d)} \tag{B.1.1}$$

$$Y_t = \qquad y_{21} = y_{12} = \frac{j}{Z_0 \sin(2\pi f T_d)} \tag{B.1.2}$$

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Sensitivity functions:

$$Y_{iz} = \frac{\partial Y_i}{\partial Z_0} = \frac{-Y_i}{Z_0} \tag{B.1.3}$$

$$Y_{tz} = \frac{\partial Y_t}{\partial Z_0} = \frac{-Y_t}{Z_0} \tag{B.1.4}$$

$$Y_{iT} = \frac{\partial Y_i}{\partial T_d} = \frac{2\,j\,\pi\,f\sec\left(2\,\pi\,f\,T_d\right)^2}{\tan\left(2\,\pi\,f\,T_d\right)^2 Z_0} \tag{B.1.5}$$

$$Y_{tT} = \frac{\partial Y_t}{\partial T_d} = \frac{-2\,j\,\pi\,f\cos\left(2\,\pi\,f\,T_d\right)}{\sin\left(2\,\pi\,f\,T_d\right)^2 Z_0} \tag{B.1.6}$$

```
# Port parameters y11 or y22
def Yi(f,Z0,Td):
    Y = -(0.0+1.0J)/Z0 / tan(2*pi*f*Td)
    return Y
#Voltage Controlled Current Sources - y12 and y21
def Yt(f,Z0,Td):
    Y = (0.0+1.0J)/Z0  / sin(2*pi*f*Td)
    return Y
#Derivatives
def Yi_z(f,Z0,Td):
    Y_z = -Yi(f,Z0,Td)/Z0
    return Y_z
def Yt_z(f,Z0,Td):
    Y_z = -Yt(f,Z0,Td)/Z0
    return Y_z
def Yi_T(f,Z0,Td):
    Y_T = (0.0+2J)*pi*f/(cos(2*pi*f*Td))**2/(tan(2*pi*f*Td))**2 /Z0
    return Y_T
def Yt_T(f,Z0,Td):
    Y_T = -(0.0+2J)*pi*f*cos(2*pi*f*Td)/(sin(2*pi*f*Td))**2 /Z0
    return Y_T
```

B.1.10 Vectors, input and output

The input vector denotes the input port where a current of 40 mA is applied.

The output vector b has two columns. Column 0 is for a first output node voltage and column 1 for a second output node voltage.

```
nodes = extractParams(l,1)[1]
print(nodes)
input_node = extractParams(l,1)[11]
```

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```
output_nodes = extractParams(1,1)[10]
I = np.zeros((nodes,1),float)
I[int(input_node)-1,0]=0.04
b = np.zeros((nodes,2),int)
b[int(output_nodes[0])-1,0]=1
b[int(output_nodes[1])-1,1]=1
print "I",I
print "b", b
```

```
7
I [[ 0.04]
 [ 0.  ]
 [ 0.  ]
 [ 0.  ]
 [ 0.  ]
 [ 0.  ]
 [ 0.  ]]
b [[1 0]
 [0 0]
 [0 0]
 [0 0]
 [0 1]
 [0 0]
 [0 0]]
```

```
def Rrange():
    return np.array([1000])
    #return np.array([1,5,18,60,150,180])
print(len(Rrange()))
```

```
1
```

B.2 Define square root sensitivities

```
P1 = np.zeros([len(Rrange())],float)
P2 = np.zeros([len(Rrange())],float)
P3 = np.zeros([len(Rrange())],float)
P4 = np.zeros([len(Rrange())],float)
P5 = np.zeros([len(Rrange())],float)
P6 = np.zeros([len(Rrange())],float)
P7 = np.zeros([len(Rrange())],float)
P8 = np.zeros([len(Rrange())],float)
```

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B.3 Analysis

```
def solveSens(Rd,Rindex):
    branches = extractParams(1,Rd)[2]
    nodes = extractParams(1,Rd)[1]
    R = extractParams(1,Rd)[3]
    C = extractParams(1,Rd)[4]
    L = extractParams(1,Rd)[5]
    T = extractParams(1,Rd)[6]
    G = extractParams(1,Rd)[7]
    Rmat = admittanceMatrices(branches,R,C,L)[0]
    Cmat = admittanceMatrices(branches,R,C,L)[1]
    Lmat = admittanceMatrices(branches,R,C,L)[2]
    Tmat = admittanceMatrices(branches,R,C,L)[3]
    A = setupIncidenceMatrix(R,C,L,T,G,nodes,branches)
    Gmat=np.zeros((branches,branches),float)
    for r in range(len(G)):
        Gmat[(G[r][1]-1,G[r][0]-1)]= G[r][6]

    for fi in findex:
        f=frange[fi]
        #Setup transmission line branch admittance matrix
        for r in range(len(T)):
            Y1=Yi(f,T[r][6],T[r][7])
            Y2=Yt(f,T[r][6],T[r][7])
            Tmat[T[r][0]-1,T[r][0]-1]=Y1
            Tmat[T[r][1]-1,T[r][1]-1]=Y1
            Tmat[T[r][0]-1,T[r][1]-1]=Y2
            Tmat[T[r][1]-1,T[r][0]-1]=Y2
        #Setup branch admittance matrix
        Yb=Rmat + 1j*2*pi*f*Cmat + 1/(1j*2*pi*f)*Lmat + Tmat + Gmat
        #Setup and solve nodal equations
        Y = np.dot(np.dot(A,Yb),A.T)
        V = np.linalg.solve(Y,I)
        #if f == 1.3e9:
         #    P1[Rindex] = (np.abs(V[0])**2)/50
          #   P2[Rindex] = (np.abs(V[1]-V[2])**2)/Rd
           # P3[Rindex] = (np.abs(V[1])**2)/50
            # P4[Rindex] = (np.abs(V[3]-V[4])**2)/Rd
            # P5[Rindex] = (np.abs(V[6]-V[7])**2)/Rd
            # P6[Rindex] = (np.abs(V[8]-V[9])**2)/Rd
            # P7[Rindex] = (np.abs(V[8])**2)/50
            # P8[Rindex] = (np.abs(V[7])**2)/50
```

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```
Vout[:,fi,0,Rindex] = np.dot(b.T,V)[:,0]
#calculate the two adjoint vectors (for the two output nodes)
a = np.linalg.solve(Y.T,b)
# Calculate sensitivities for resistors
for r in range(len(R)):
    #Reset derivatives of branch admittance arrays
    Rmats = np.zeros((branches,branches),float)
    Rmats[R[r][0]-1,R[r][0]-1]=-1/(R[r][3]**2)
    Y = np.dot(np.dot(A,Rmats),A.T)
    Vout_R[:,fi,r,Rindex] = np.dot(-np.dot(a.T,Y),V)[:,0]
    #normalise for sensitivity
    Sout_R[:,fi,r,Rindex]=R[r][3]*Vout_R[:,fi,r,Rindex]/\
                          Vout[:,fi,0,Rindex]
# Calculate sensitivities for capacitors
for r in range(len(C)):
    Cmats = np.zeros((branches,branches),int)
    Cmats[C[r][0]-1,C[r][0]-1]=1
    Y = np.dot(np.dot(A,1j*2*pi*f*Cmats),A.T)
    Vout_C[:,fi,r,Rindex] = np.dot(-np.dot(a.T,Y),V)[:,0]
    #normalise for sensitivity
    Sout_C[:,fi,r,Rindex]=C[r][3]*Vout_C[:,fi,r,Rindex]/\
                          Vout[:,fi,0,Rindex]
for r in range(len(L)):
    Lmats = np.zeros((branches,branches),float)
    Lmats[L[r][0]-1,L[r][0]-1]=-1/(L[r][3]**2)
    Y = np.dot(np.dot(A,1/(1j*2*pi*f)*Lmats),A.T)
    Vout_L[:,fi,r,Rindex] = np.dot(-np.dot(a.T,Y),V)[:,0]
    #normalise for sensitivity
    Sout_L[:,fi,r,Rindex]=L[r][3]*Vout_L[:,fi,r,Rindex]/\
                          Vout[:,fi,0,Rindex]
for r in range(len(T)):
    Tmats = np.zeros((branches,branches),complex)
    Y1=Yi_z(f,T[r][6],T[r][7])
    Y2=Yt_z(f,T[r][6],T[r][7])
    Tmats[T[r][0]-1,T[r][0]-1]=Y1
    Tmats[T[r][1]-1,T[r][1]-1]=Y1
    Tmats[T[r][0]-1,T[r][1]-1]=Y2
    Tmats[T[r][1]-1,T[r][0]-1]=Y2
    Y = np.dot(np.dot(A,Tmats),A.T)
    Vout_Tz[:,fi,r,Rindex] = np.dot(-np.dot(a.T,Y),V)[:,0]
    #normalise for sensitivity
    Sout_Tz[:,fi,r,Rindex]=T[r][6]*Vout_Tz[:,fi,r,Rindex]/\
                           Vout[:,fi,0,Rindex]
for r in range(len(T)):
```

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```
                Tmats = np.zeros((branches,branches),complex)
                Y1=Yi_T(f,T[r][6],T[r][7])
                Y2=Yt_T(f,T[r][6],T[r][7])
                Tmats[T[r][0]-1,T[r][0]-1]=Y1
                Tmats[T[r][1]-1,T[r][1]-1]=Y1
                Tmats[T[r][0]-1,T[r][1]-1]=Y2
                Tmats[T[r][1]-1,T[r][0]-1]=Y2
                Y = np.dot(np.dot(A,Tmats),A.T)
                Vout_TT[:,fi,r,Rindex] = np.dot(-np.dot(a.T,Y),V)[:,0]
                #normalise for sensitivity
                Sout_TT[:,fi,r,Rindex]=T[r][7]*Vout_TT[:,fi,r,Rindex]/\
                                        Vout[:,fi,0,Rindex]
                #if frange[fi] == 1.2e9:
                    #print(T[r][7],Sout_TT[:,fi,r,Rindex], Vout[:,fi,0])
        # Sensitivity for VCCS
            for r in range(len(G)):
                Gmats = np.zeros((branches,branches),int)
                Gmats[(G[r][1]-1,G[r][0]-1)]= 1
                Y = np.dot(np.dot(A,Gmats),A.T)
                Vout_G[:,fi,r,Rindex] = np.dot(-np.dot(a.T,Y),V)[:,0]
                #normalise for sensitivity
                Sout_G[:,fi,r,Rindex]=G[r][6]*Vout_G[:,fi,r,Rindex]/\
                                        Vout[:,fi,0,Rindex]
        return R,C,L,T,len(G)
```

B.4 Group RSS sensitivities per element type

```
def RSSsens(Rindex,Rlen,Clen,Llen,Tlen,Glen):
    for r in range(Rlen):
        Sout_Rsqrt[:,0,Rindex] = Sout_Rsqrt[:,0,Rindex] + np.power\
            (np.real(Sout_R[1,:,r,Rindex]),2)
        Sout_Rsqrt[:,1,Rindex] = Sout_Rsqrt[:,1,Rindex] + np.power\
            (np.imag(Sout_R[1,:,r,Rindex])*180/pi,2)
        Sout_Rsqrt[:,2,Rindex] = Sout_Rsqrt[:,2,Rindex] + np.power\
            (np.real(Sout_R[0,:,r,Rindex]),2)
        Sout_Rsqrt[:,3,Rindex] = Sout_Rsqrt[:,3,Rindex] + np.power\
            (np.imag(Sout_R[0,:,r,Rindex])*180/pi,2)

    for l in range(0,Llen):
        Sout_Lsqrt[:,0,Rindex] = Sout_Lsqrt[:,0,Rindex] + np.power\
            (np.real(Sout_L[1,:,l,Rindex]),2)
        Sout_Lsqrt[:,1,Rindex] = Sout_Lsqrt[:,1,Rindex] + np.power\
            (np.imag(Sout_L[1,:,l,Rindex])*180/pi,2)
        Sout_Lsqrt[:,2,Rindex] = Sout_Lsqrt[:,2,Rindex] + np.power\
```

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```
            (np.real(Sout_L[0,:,1,Rindex]),2)
        Sout_Lsqrt[:,3,Rindex] = Sout_Lsqrt[:,3,Rindex] + np.power\
            (np.imag(Sout_L[0,:,1,Rindex])*180/pi,2)

    for c in range(Clen):
        Sout_Csqrt[:,0,Rindex] = Sout_Csqrt[:,0,Rindex] + np.power\
            (np.real(Sout_C[1,:,c,Rindex]),2)
        Sout_Csqrt[:,1,Rindex] = Sout_Csqrt[:,1,Rindex] + np.power\
            (np.imag(Sout_C[1,:,c,Rindex])*180/pi,2)
        Sout_Csqrt[:,2,Rindex] = Sout_Csqrt[:,2,Rindex] + np.power\
            (np.real(Sout_C[0,:,c,Rindex]),2)
        Sout_Csqrt[:,3,Rindex] = Sout_Csqrt[:,3,Rindex] + np.power\
            (np.imag(Sout_C[0,:,c,Rindex])*180/pi,2)

    for tz in range(Tlen):
        Sout_Tzsqrt[:,0,Rindex] = Sout_Tzsqrt[:,0,Rindex] + \
                                  Sout_Tz[1,:,tz,Rindex]
        Sout_Tzsqrt[:,1,Rindex] = Sout_Tzsqrt[:,1,Rindex] + \
                                  Sout_Tz[0,:,tz,Rindex]


    for tt in range(Tlen):
        Sout_Ttsqrt[:,0,Rindex] = Sout_Ttsqrt[:,0,Rindex] + \
                                  Sout_TT[1,:,tt,Rindex]
        Sout_Ttsqrt[:,1,Rindex] = Sout_Ttsqrt[:,1,Rindex] + \
                                  Sout_TT[0,:,tt,Rindex]

    return
```

B.5 Calculate total RSS sensitivity

```
def RSStotal(Rindex):
    Sout_Z0epse = -1 / 2 * np.ones(len(frange))
    Sout_Tdepse = 1 / 2 * np.ones(len(frange))
    Sout_Z0h = 0.63536 * np.ones(len(frange))
    Sepse_epsr = 0.89133 * np.ones(len(frange))
    wR = 0.1 * np.ones(len(frange))
    wC = 0.1 * np.ones(len(frange))
    wL = 0.1 * np.ones(len(frange))
    weps = 0.015 * np.ones(len(frange))
    wh = 0.07 * np.ones(len(frange))
    print(Stotal[1,0,Rindex])
    Stotal[:, 0,Rindex] = np.sqrt(Sout_Rsqrt[:, 0,Rindex]
                          * wR ** 2 + Sout_Lsqrt[:, 0,Rindex]
```

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```
                        * wL ** 2 + Sout_Csqrt[:, 0,Rindex]
                        * wC ** 2 + np.power(np.real(
        (Sout_Tzsqrt[:, 0,Rindex] * Sout_Z0epse * Sepse_epsr +
                                Sout_Ttsqrt[:, 0,Rindex]
         *Sout_Tdepse * Sepse_epsr))* weps, 2) + np.power
            (np.real(( Sout_Tzsqrt[:, 0,Rindex]* Sout_Z0h))
             * wh, 2)) #
    Stotal[:, 1,Rindex] = np.sqrt(Sout_Rsqrt[:, 1,Rindex]
                        * wR ** 2 + Sout_Lsqrt[:, 1,Rindex]
                        * wL ** 2 + Sout_Csqrt[:, 1,Rindex]
                        * wC ** 2 + np.power(np.imag(
        (Sout_Tzsqrt[:, 0,Rindex] * Sout_Z0epse * Sepse_epsr +
        Sout_Ttsqrt[:, 0,Rindex] * Sout_Tdepse * Sepse_epsr))
                        * weps * 180 / pi, 2) + np.power(np.imag(
        ( Sout_Tzsqrt[:, 0,Rindex] * Sout_Z0h)) * wh * 180 / pi, 2)) #
    Stotal[:, 2,Rindex] = np.sqrt(Sout_Rsqrt[:, 2,Rindex]
                        * wR ** 2 + Sout_Lsqrt[:, 2,Rindex]
                        * wL ** 2 + Sout_Csqrt[:, 2,Rindex]
                        * wC ** 2 + np.power(np.real(
        (Sout_Tzsqrt[:, 1,Rindex] * Sout_Z0epse * Sepse_epsr +
            Sout_Ttsqrt[:, 1,Rindex] * Sout_Tdepse * Sepse_epsr))
                        * weps, 2) + np.power(np.real(
        (Sout_Tzsqrt[:, 1,Rindex]* Sout_Z0h)) * wh, 2)) #
    Stotal[:, 3,Rindex] = np.sqrt(Sout_Rsqrt[:, 3,Rindex]
                        * wR ** 2 + Sout_Lsqrt[:, 3,Rindex]
                        * wL ** 2 + Sout_Csqrt[:, 3,Rindex]
                        * wC ** 2 + np.power(np.imag(
        (Sout_Tzsqrt[:, 1,Rindex] * Sout_Z0epse * Sepse_epsr +
        Sout_Ttsqrt[:, 1,Rindex] * Sout_Tdepse * Sepse_epsr))
                        * weps * 180 / pi,2) + np.power(np.imag(
        (Sout_Tzsqrt[:, 1,Rindex] * Sout_Z0h))* wh * 180 / pi , 2)) #
    STztotal[:,0,Rindex] = np.real((Sout_Ttsqrt[:, 0,Rindex]
                                    * Sout_Tdepse))* weps
    STztotal[:,1,Rindex] = np.imag((Sout_Ttsqrt[:, 0,Rindex]
                                    * Sout_Tdepse)) * weps * 180 / pi
    STztotal[:,2,Rindex] = np.real((Sout_Ttsqrt[:, 1,Rindex]
                                    * Sout_Tdepse)) * weps
    STztotal[:,3,Rindex] = np.imag((Sout_Ttsqrt[:, 1,Rindex]
                                    * Sout_Tdepse)) * weps * 180 / pi
    return

findex = extractParams(1,1)[8]
frange = extractParams(1,1)[9]
Vout = np.zeros((2,len(findex),1,len(Rrange())),complex)
```

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```
Vout_R = np.zeros((2,len(findex),len(extractParams(1,1)[3])
                        ,len(Rrange())),complex)
Sout_R = np.zeros((2,len(findex),len(extractParams(1,1)[3])
                        ,len(Rrange())),complex)
deltaOut_R = np.zeros((2,len(findex),len(extractParams(1,1)[3])
                          ,len(Rrange())),complex)
Vout_C = np.zeros((2,len(findex),len(extractParams(1,1)[4])
                        ,len(Rrange())),complex)
Sout_C = np.zeros((2,len(findex),len(extractParams(1,1)[4])
                        ,len(Rrange())),complex)
Vout_L = np.zeros((2,len(findex),len(extractParams(1,1)[5])
                        ,len(Rrange())),complex)
Sout_L = np.zeros((2,len(findex),len(extractParams(1,1)[5])
                        ,len(Rrange())),complex)
Vout_Tz = np.zeros((2,len(findex),len(extractParams(1,1)[6])
                         ,len(Rrange())),complex)
Sout_Tz = np.zeros((2,len(findex),len(extractParams(1,1)[6])
                         ,len(Rrange())),complex)
Vout_TT = np.zeros((2,len(findex),len(extractParams(1,1)[6])
                         ,len(Rrange())),complex)
Sout_TT = np.zeros((2,len(findex),len(extractParams(1,1)[6])
                         ,len(Rrange())),complex)
Vout_G = np.zeros((2,len(findex),len(extractParams(1,1)[7])
                        ,len(Rrange())),complex)
Sout_G = np.zeros((2,len(findex),len(extractParams(1,1)[7])
                        ,len(Rrange())),complex)
Sout_Rsqrt = np.zeros([len(frange),4,len(Rrange())])
Sout_Lsqrt = np.zeros([len(frange),4,len(Rrange())])
Sout_Csqrt = np.zeros([len(frange),4,len(Rrange())])
Sout_Tzsqrt = np.zeros([len(frange),2,len(Rrange())],complex)
Sout_Ttsqrt = np.zeros([len(frange),2,len(Rrange())],complex)
STztotal= np.zeros([len(frange), 4, len(Rrange())])
Stotal = np.zeros([len(frange), 4, len(Rrange())])
for Rindex in range(0,len(Rrange())):
    R,C,L,T,Glen = solveSens(Rrange()[Rindex],Rindex)
    RSSsens(Rindex,len(R),len(C),len(L),len(T),Glen)
    results_dir = os.path.dirname(fnl + "/")
    RSStotal(Rindex)
    #plotR(Rindex,R)
    #plotC(Rindex,C)
    #plotL(Rindex,L)
    #plotTT(Rindex,T)
    #plotTZ(Rindex,T)
    #plotS11(Rindex,T)
```

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```
    #plotCS11(Rindex,C)
plotS21S11()
#plotRSS()
#print(Stotal[len(frange)/2, 1, :])
#plotPower()

0.0

def plotPower():
    fig, ax = plt.subplots(1, 1, figsize=(2.5, 1.8))
    #ax.plot(Rrange(),P1/0.02,label='$R_{1}$')
    ax.plot(Rrange(),P2/0.02,label='$R_{d1}$')
    ax.plot(Rrange(),P3/0.02,label='$R_{2}$')
    ax.plot(Rrange(),P4/0.02,label='$R_{d2}$')
    ax.plot(Rrange(),P5/0.02,label='$R_{d3}$')
    ax.plot(Rrange(),P6/0.02,label='$R_{d4}$')
    ax.plot(Rrange(),P7/0.02,label='$R_{3}$')
    ax.plot(Rrange(),P8/0.02,label='$R_{4}$')
    ax.grid()
    ax.legend()
    ax.set_ylabel("Normalised Power (W/W)")
    ax.set_xlabel("Equivalent Resistance ($\Omega$)")
    fig.savefig(results_dir+"/RvsP"+fnl+".svg", format='svg')
    return

def plotRSS():
    plt.figure(1, figsize=(2.5, 1.8))
    for i in range(len(Rrange())):
        plt.plot(frange, np.abs(Vout[1, :, 0, i]),label='Rd = '
                                        + str(Rrange()[i]))
    plt.grid()
    plt.legend()
    plt.ylabel("Vout")
    plt.xlabel("Frequency (GHz)")
    plt.savefig(results_dir+"/Vout"+fnl+"mag.svg", format='svg')
    plt.close()
    plt.figure(2,figsize=(2.5,1.8))
    for i in range(len(Rrange())):
        plt.plot(frange, Stotal[:, 0, i],label='Rd = '
                                        + str(Rrange()[i]))
    plt.grid()
    plt.legend()
    plt.ylabel("RSS magnitude error")
    plt.xlabel("Frequency (GHz)")
    #fig.show()
```

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```
    plt.savefig(results_dir+"/RSSerror"+fnl+"mag.svg"
                , format='svg')
    plt.figure(3, figsize=(2.5, 1.8))
    for i in range(len(Rrange())):
        plt.plot(frange, np.angle(Vout[1, :, 0, i],deg=True),
                 label='Rd = '+ str(Rrange()[i])+ r'$\Omega $')
    plt.grid()
    plt.legend()
    plt.ylabel("Phase(Vout) ")
    plt.xlabel("Frequency (GHz)")
    plt.savefig(results_dir+"/Vout"+fnl+"phase.svg", format='svg')
    plt.close()
    plt.figure(4,figsize=(2.5,1.8))
    for i in range(len(Rrange())):
        plt.plot(frange, Stotal[:, 1, i],
                 label='Rd = '+ str(Rrange()[i])+ r'$\Omega $')
    plt.grid()
    plt.legend()
    plt.ylabel("RSS phase error")
    plt.xlabel("Frequency (GHz)")
    plt.savefig(results_dir+"/RSSerror"+fnl+"phase.svg", format='svg')
    plt.close()
    #fig.show()
    return
```

B.5.1 Results

B.5.1.1 Amplitude Response and amplitude sensitivities

```
def plotS21S11():
    plt.figure(1, figsize=(2.5, 1.8))
    for i in range(len(Rrange())):
        plt.plot(frange,20*np.log10(np.abs(Vout[1,:,0,i]))
                 ,label='Rd ='+ str(Rrange()[i]))
    plt.grid()
    plt.legend()
    plt.ylabel('|S21| (dB)')
    plt.xlabel('Frequency (GHz)')
    plt.savefig(results_dir+"/"+fnl+"S21dB.svg", format='svg')
    plt.close()
    plt.figure(2,figsize=(2.5,1.8))
    for i in range(len(Rrange())):
        plt.plot(frange,20*np.log10(np.abs(Vout[0,:,0,i]-1))
                 ,label='Rd =' + str(Rrange()[i]))
    plt.grid()
```

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```
    plt.legend()
    plt.xlabel('Frequency (GHz)')
    plt.ylabel('|S11|  (dB)')
    plt.savefig(results_dir+"/"+fnl+"S11dB.svg", format='svg')
    plt.close()
    return
```

B.5.1.2 R sensitivities

```
def plotR(Rindex,R):
    fig,ax =plt.subplots(2,2, figsize=(5,3.5))
    ax[0,0].plot(frange,np.abs(Vout[1,:,0,Rindex])
                 , label='|Vout| = '+ str(np.round(
            np.abs(Vout[1,300,0,Rindex]),2))+ 'V')
    ax[0,0].grid()
    ax[0,0].set_ylabel("|Vout| (V)")
    ax[0,0].legend()
    ax[0,1].plot(frange,(np.abs(Vout[0,:,0,Rindex]))
                 , label='|Vin| = ' + str(np.round(
            np.abs(Vout[0,300,0,Rindex]),2))+ ' V')
    ax[0,1].grid()
    ax[0,1].set_ylabel("|Vin| (V)")
    ax[0,1].legend()
    for r in range(len(R)):
        ax[1,0].plot(frange,np.real(Sout_R[1,:,r,Rindex])
                     ,label=(R[r][4]))
    ax[1,0].grid()
    ax[1,0].set_xlabel("Frequency (GHz)")
    ax[1,0].set_ylabel("Sens(|Vout|) wrt R")
    ax[1,0].legend()
    for r in range(len(R)):
        ax[1,1].plot(frange,np.real(Sout_R[0,:,r,Rindex])
                     ,label=(R[r][4]))
    ax[1,1].grid()
    ax[1,1].set_xlabel("Frequency (GHz)")
    ax[1,1].set_ylabel("Sens(|Vin|) wrt R")
    ax[1,1].legend()
    fig.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"_mag_R.svg", format='svg')
    ##########################################################################
    # Phase sensitivities
    fig,ax = plt.subplots(2,2, figsize=(5, 3.5))
    ax[0,0].plot(frange,np.angle(Vout[1,:,0,Rindex],deg=True)
                 ,label='Phase(Vout) ='+ str(np.round(
```

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```
            np.angle(Vout[1,300,0,Rindex],deg=True),2))+'$^o$')
    ax[0,0].grid()
    ax[0,0].legend()
    ax[0,0].set_ylabel("Phase(Vout) (Degrees)")
    ax[0,1].plot(frange,(np.angle(Vout[0,:,0,Rindex]
                ,deg=True)), label='Phase(Vin) ='
                + str(np.round(np.angle(Vout[0,300,0,Rindex]
                                        ,deg=True),2))+'$^o$')
    ax[0,1].grid()
    ax[0,1].legend()
    ax[0,1].set_ylabel("Phase(Vin) (Degrees)")
    for r in range(len(R)):
        ax[1,0].plot(frange,np.imag(Sout_R[1,:,r,Rindex])
                    *180/pi,label=(R[r][4]))
    ax[1,0].grid()
    ax[1,0].set_xlabel("Frequency (GHz)")
    ax[1,0].set_ylabel("Sens Phase(Vout) wrt R")
    ax[1,0].legend()
    for r in range(len(R)):
        ax[1,1].plot(frange,np.imag(Sout_R[0,:,r,Rindex])
                    *180/pi,label=(R[r][4]))
    ax[1,1].grid()
    ax[1,1].set_xlabel("Frequency (GHz) ")
    ax[1,1].set_ylabel("Sens Phase(Vin) wrt R")
    ax[1,1].legend()
    fig.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"_Sens_phase_R.svg",format='svg')
    return
```

B.5.1.3 C sensitivities

```
def plotC(Rindex,C):
    fig, ax = plt.subplots(2, 2, figsize=(5, 3.5))
    ax[0,0].plot(frange,np.abs(Vout[1,:,0,Rindex])
                , label='|Vout| = ' + str(np.round(
            np.abs(Vout[1,300,0,Rindex]),2))+ 'V')
    ax[0,0].grid()
    ax[0,0].legend()
    ax[0,0].set_ylabel("Vout")
    ax[0,1].plot(frange,(np.abs(Vout[0,:,0,Rindex]))
                , label='|Vin| = '+ str(np.round(
            np.abs(Vout[0,300,0,Rindex]),2))+ 'V')
    ax[0,1].grid()
    ax[0,1].legend()
```

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```
ax[0,1].set_ylabel("Vin")
for r in range(len(C)):
    ax[1,0].plot(frange,np.real(Sout_C[1,:,r,Rindex])
                 ,label=(C[r][4]))
ax[1,0].grid()
ax[1,0].set_xlabel("Frequency  (GHz)")
ax[1,0].set_ylabel("Sens(|Vout|) wrt C")
ax[1,0].legend()
for r in range(len(C)):
    ax[1,1].plot(frange,np.real(Sout_C[0,:,r,Rindex])
                 ,label=(C[r][4]))
ax[1,1].grid()
ax[1,1].set_xlabel("Frequency (GHz)")
ax[1,1].set_ylabel("Sens(|Vin|) wrt C")
ax[1,1].legend()
plt.savefig(results_dir+"/"+str(Rrange()[Rindex])
            +fnl+"_mag_C.svg", format='svg')
#fig.close()
fig, ax = plt.subplots(2, 2, figsize=(5, 3.5))
ax[0,0].plot(frange,np.angle(Vout[1,:,0,Rindex],deg=True)
             , label='Phase(Vout) = '+ str(np.round(
        np.angle(Vout[1,300,0,Rindex],deg=True),2))+ '$^o$')
ax[0,0].grid()
ax[0,0].legend()
ax[0,0].set_ylabel("Phase(Vout) (Degrees)")
ax[0,1].plot(frange,(np.angle(Vout[0,:,0,Rindex]
                     ,deg=True)), label='Phase(Vin) = '
                + str(np.round(np.angle(Vout[0,300,0,Rindex]
                ,deg=True),2))+ '$^o$')
ax[0,1].grid()
ax[0,1].legend()
ax[0,1].set_ylabel("Phase(Vin) (Degrees)")
for r in range(len(C)):
    ax[1,0].plot(frange,np.imag(Sout_C[1,:,r,Rindex])
                 *180/pi,label=(C[r][4]))
ax[1,0].grid()
ax[1,0].set_xlabel("Frequency (GHz)")
ax[1,0].set_ylabel("Sens Phase(Vout) wrt C")
ax[1,0].legend()
for r in range(len(C)):
    ax[1,1].plot(frange,np.imag(Sout_C[0,:,r,Rindex])
                 *180/pi,label=(C[r][4]))
ax[1,1].grid()
ax[1,1].set_xlabel("Frequency (GHz)")
```

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```
    ax[1,1].set_ylabel("Sens Phase(Vin) wrt C")
    ax[1,1].legend()
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"_phase_C.svg")
    #fig.close()
    return

def plotCS11(Rindex,C):
    plt.figure(1,figsize=(2.5,1.8))
    for r in range(len(C)):
        plt.plot(frange,np.real(Sout_C[0,:,r,Rindex]*
                 Vout[0,:,0,Rindex]/(Vout[0,:,0,Rindex]-1))
                  ,label=(C[r][4]))
    plt.grid()
    plt.legend()
    plt.xlabel("Frequency  (GHz)")
    plt.ylabel("Sens(|S11|) wrt C")
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"S11_sens_C.svg")
    plt.close()
    return
```

B.5.1.4 L sensitivities

```
def plotL(Rindex,L):
    fig, ax = plt.subplots(2, 2, figsize=(5, 3.5))
    ax[0,0].plot(frange,np.abs(Vout[1,:,0,Rindex])
                  , label='|Vout| = '+ str(np.round(
            np.abs(Vout[1,300,0,Rindex]),2))+ 'V')
    ax[0,0].grid()
    ax[0,0].legend()
    ax[0,0].set_ylabel("|Vout| (V)")
    ax[0,1].plot(frange,(np.abs(Vout[0,:,0,Rindex]))
                  , label='|Vin| = '+ str(np.round(
            np.abs(Vout[0,300,0,Rindex]),2))+ 'V')
    ax[0,1].grid()
    ax[0,1].legend()
    ax[0,1].set_ylabel("|Vin| (V)")
    for r in range(len(L)):
        ax[1,0].plot(frange,np.real(Sout_L[1,:,r,Rindex])
                     ,label=(L[r][4]))
    ax[1,0].grid()
    ax[1,0].set_xlabel("Frequency (GHz)")
    ax[1,0].set_ylabel("Sens |Vout| wrt L")
    ax[1,0].legend()
```

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```
    for r in range(len(L)):
        ax[1,1].plot(frange,np.real(Sout_L[0,:,r,Rindex])
                     ,label=(L[r][4]))
    ax[1,1].grid()
    ax[1,1].set_xlabel("Frequency (GHz)")
    ax[1,1].set_ylabel("Sens |Vin| wrt L")
    ax[1,1].legend()
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"_mag_L.svg", format='svg')
    #fig.close()
    fig, ax = plt.subplots(2, 2, figsize=(5, 3.5))
    ax[0,0].plot(frange,np.angle(Vout[1,:,0,Rindex],deg=True)
                 , label='Phase(Vout) = '+ str(np.round(
              np.angle(Vout[1,300,0,Rindex],deg=True),2))+  '$^o$')
    ax[0,0].grid()
    ax[0,0].legend()
    ax[0,0].set_ylabel("Phase(Vout) (Degrees)")
    ax[0,1].plot(frange,(np.angle(Vout[0,:,0,Rindex]
                 ,deg=True)), label='Phase(Vin) = '
                + str(np.round(np.angle(Vout[0,300,0,Rindex]
                 ,deg=True),2))+  '$^o$')
    ax[0,1].grid()
    ax[0,1].legend()
    ax[0,1].set_ylabel("Phase(Vin) (Degrees)")
    for r in range(len(L)):
        ax[1,0].plot(frange,np.imag(Sout_L[1,:,r,Rindex])
                     *180/pi,label=(L[r][4]))
    ax[1,0].grid()
    ax[1,0].set_xlabel("Frequency (GHz)")
    ax[1,0].set_ylabel("Sens Phase(Vout) wrt L")
    ax[1,0].legend()
    for r in range(len(L)):
        ax[1,1].plot(frange,np.imag(Sout_L[0,:,r,Rindex])
                     *180/pi,label=(L[r][4]))
    ax[1,1].grid()
    ax[1,1].set_xlabel("Frequency (GHz)")
    ax[1,1].set_ylabel("Sens Phase(S11) wrt L ")
    ax[1,1].legend()
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"_phase_L.svg")
    #fig.close()
    return
```

B.5.1.5 T sensitivities for Z_0

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```
def plotTZ(Rindex,T):
    fig, ax = plt.subplots(2, 2, figsize=(5, 3.5))
    ax[0,0].plot(frange,np.abs(Vout[1,:,0,Rindex])
                 , label='|Vout| = '+ str(np.round(
            np.abs(Vout[1,300,0,Rindex]),2))+ 'V')
    ax[0,0].grid()
    ax[0,0].legend()
    ax[0,0].set_xlabel("Frequency (GHz)")
    ax[0,0].set_ylabel("|Vout| (V)")
    ax[0,1].plot(frange,(np.abs(Vout[0,:,0,Rindex]))
            , label='|Vin| = '+ str(np.round(
            np.abs(Vout[0,300,0,Rindex]),2))+ 'V')
    ax[0,1].grid()
    ax[0,1].legend()
    ax[0,1].set_xlabel("Frequency (GHz)")
    ax[0,1].set_ylabel("|Vin| (V)")
    for r in range(len(T)):
        ax[1,0].plot(frange,np.real(Sout_Tz[1,:,r,Rindex])
                     ,label=(T[r][8]))
    ax[1,0].grid()
    ax[1,0].set_xlabel("Frequency (GHz)")
    ax[1,0].set_ylabel("Sens(|Vout|) wrt TL Z0")
    ax[1,0].legend()
    for r in range(len(T)):
        ax[1,1].plot(frange,np.real(Sout_Tz[0,:,r,Rindex])
                     ,label=(T[r][8]))
    ax[1,1].grid()
    ax[1,1].set_xlabel("Frequency (GHz)")
    ax[1,1].set_ylabel("Sens(|Vin|) wrt TL Z0")
    ax[1,1].legend()
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"_mag_T_Z0.svg", format='svg')
    #fig.close()
    fig, ax = plt.subplots(2, 2, figsize=(5, 3.5))
    ax[0,0].plot(frange,np.angle(Vout[1,:,0,Rindex],deg=True)
                 , label='Phase(Vout) = '
                + str(np.round(np.angle(Vout[1,300,0,Rindex]
                                        ,deg=True),2))+ '$^o$')
    ax[0,0].grid()
    ax[0,0].legend()
    ax[0,0].set_xlabel("Frequency (GHz)")
    ax[0,0].set_ylabel("Phase(Vout) (Degrees)")
    ax[0,1].plot(frange,(np.angle(Vout[0,:,0,Rindex],deg=True))
                 , label='Phase(Vin) = '
```

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```
                + str(np.round(np.angle(Vout[0,300,0,Rindex]
                                        ,deg=True),2))+ '$^o$')
    ax[0,1].grid()
    ax[0,1].legend()
    ax[0,1].set_xlabel("Frequency (GHz)")
    ax[0,1].set_ylabel("Phase(Vin) (Degrees)")
    for r in range(len(T)):
        ax[1,0].plot(frange,np.imag(Sout_Tz[1,:,r,Rindex])
                     *180/pi,label=(T[r][8]))
    ax[1,0].grid()
    ax[1,0].set_xlabel("Frequency (GHz)")
    ax[1,0].set_ylabel("Sens Phase(Vout) wrt TL Z0")
    ax[1,0].legend()
    for r in range(len(T)):
        ax[1,1].plot(frange,np.imag(Sout_Tz[0,:,r,Rindex])
                     *180/pi,label=(T[r][8]))
    ax[1,1].grid()
    ax[1,1].set_xlabel("Frequency (GHz)")
    ax[1,1].set_ylabel("Sens Phase(Vin) wrt TL Z0")
    ax[1,1].legend()
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"_phase_T_Z0.svg")
    #fig.close()
    return
```

B.5.1.6 T sensitivities for T_d

```
def plotTT(Rindex,T):
    fig, ax = plt.subplots(2, 2, figsize=(5, 3.5))
    ax[0,0].plot(frange,np.abs(Vout[1,:,0,Rindex])
                 , label='|Vout| = '+ str(np.round(
            np.abs(Vout[1,300,0,Rindex]),2))+ 'V')
    ax[0,0].grid()
    ax[0,0].legend()
    ax[0,0].set_ylabel("|Vout| (V)")
    ax[0,1].plot(frange,(np.abs(Vout[0,:,0,Rindex]))
                 , label='|Vin| = ' + str(np.round(
            np.abs(Vout[0,300,0,Rindex]),2))+ 'V')
    ax[0,1].grid()
    ax[0,1].legend()
    ax[0,1].set_ylabel("|Vin| (V)")
    for r in range(len(T)):
        ax[1,0].plot(frange,np.real(Sout_TT[1,:,r,Rindex])
                     ,label=(T[r][8]))
```

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```
ax[1,0].grid()
ax[1,0].set_xlabel("Frequency (GHz)")
ax[1,0].set_ylabel("Sens(|Vout|) wrt TL Td")
ax[1,0].legend()
for r in range(len(T)):
    ax[1,1].plot(frange,np.real(Sout_TT[0,:,r,Rindex])
                 ,label=(T[r][8]))
ax[1,1].grid()
ax[1,1].set_xlabel("Frequency (GHz)")
ax[1,1].set_ylabel("Sens(|Vin|) wrt TL Td")
ax[1,1].legend()
fig.savefig(results_dir+"/"+str(Rrange()[Rindex])
            +fnl+"_mag_T_Td.svg")
fig2, ax = plt.subplots(2, 2, figsize=(5, 3.5))
ax[0,0].plot(frange , np.angle(Vout[1, :,0,Rindex]
                , deg=True), label='Phase(Vout) = '
                + str(np.round(np.angle(Vout[1,300,0,Rindex]
                ,deg=True),2))+ '$^o$')
ax[0,0].grid()
ax[0,0].legend()
ax[0,0].set_ylabel("Phase(Vout) (Degrees)")
for r in range(len(T)):
    ax[1,0].plot(frange,np.imag(Sout_TT[1,:,r,Rindex])
                 *180/pi,label=(T[r][8]))
ax[1,0].grid()
ax[1,0].legend()
ax[1,0].set_xlabel("Frequency (GHz)")
ax[1,0].set_ylabel("Sens Phase(Vout) wrt TL Td")
ax[0,1].set_ylabel("Phase(Vin) (Degrees)")
ax[0,1].plot(frange,(np.angle(Vout[0,:,0,Rindex],deg=True))
             , label='Phase(Vin) = '+ str(np.round(
        np.angle(Vout[0,300,0,Rindex],deg=True),2))+ '$^o$')
ax[0,1].grid()
ax[0,1].legend()
for r in range(len(T)):
    ax[1,1].plot(frange,np.imag(Sout_TT[0,:,r,Rindex])
                 *180/pi,label=(T[r][8]))
ax[1,1].grid()
ax[1,1].set_xlabel("Frequency (GHz)")
ax[1,1].set_ylabel("Sens Phase(Vin) wrt TL Td")
ax[1,1].legend()
fig2.savefig(results_dir+"/"+str(Rrange()[Rindex])
             +fnl+"_phase_T_Td.svg")
return
```

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```
def plotS11(Rindex,T):
    plt.figure(1, figsize=(2.5, 1.8))
    plt.plot(frange,(np.angle(Vout[0,:,0,Rindex]-1,deg=True)),
             label='Phase(S11) @ 1.3GHz= '
        + str(np.round(np.angle(Vout[0,300,0,Rindex]-1
                                ,deg=True),2))+ '$^o$')
    plt.grid()
    plt.legend()
    plt.ylabel("Phase(S11) ($^o$)")
    plt.xlabel("Frequency (GHz)")
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex]) +fnl
                + "_phase_T_S11.svg", format='svg')
    plt.close()

    plt.figure(2, figsize=(2.5,1.8))
    for r in range(len(T)):
        plt.plot(frange,np.imag(Sout_TT[0,:,r,Rindex]*
            Vout[0,:,0,Rindex]/(Vout[0,:,0,Rindex]-1))
                *180/pi,label=(T[r][8]))
    plt.grid()
    plt.legend()
    plt.xlabel("Frequency (GHz)")
    plt.ylabel("Sens Phase(S11) wrt TL Td")
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"_phaseSens_T_S11.svg", format='svg')
    plt.close()

    plt.figure(3, figsize=(2.5,1.8))
    for r in range(len(T)):
        plt.plot(frange,np.imag(Sout_Tz[0,:,r,Rindex]*
            Vout[0,:,0,Rindex]/(Vout[0,:,0,Rindex]-1))
                *180/pi,label=(T[r][8]))
    plt.legend()
    plt.grid()
    plt.xlabel("Frequency (GHz)")
    plt.ylabel("Sens Phase(S11) wrt TL Z0")
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])+fnl
                +"_phaseSens_Z0_S11.svg", format='svg')
    plt.close()

    plt.figure(4, figsize=(2.5,1.8))
    for r in range(len(T)):
        plt.plot(frange,np.real(Sout_TT[0,:,r,Rindex]*
            Vout[0,:,0,Rindex]/(Vout[0,:,0,Rindex]-1))
```

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```
                ,label=(T[r][8]))
    plt.grid()
    plt.legend()
    plt.xlabel("Frequency (GHz)")
    plt.ylabel("Sens | S11 | wrt TL Td")
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])+fnl
                +"_magSens_T_S11.svg", format='svg')
    plt.close()

    plt.figure(5, figsize=(2.5,1.8))
    for r in range(len(T)):
        plt.plot(frange,np.real(Sout_Tz[0,:,r,Rindex]*
            Vout[0,:,0,Rindex]/(Vout[0,:,0,Rindex]-1))
                ,label=(T[r][8]))
    plt.grid()
    plt.legend()
    plt.xlabel("Frequency (GHz)")
    plt.ylabel("Sens | S11 | wrt TL Z0")
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])+fnl
                +"_magSens_Z0_S11.svg", format='svg')
    plt.close()

    custom_ntwk = rf.Network(f = frange
                        , s= Vout[0,:,0,Rindex]-1, z0=50)
    plt.figure(6,figsize=(2.5,1.8))
    plt.grid()
    plt.legend()
    custom_ntwk.plot_s_smith(marker = 'o', markevery=300)
    plt.savefig(results_dir+"/"+str(Rrange()[Rindex])
                +fnl+"_smith_T_S11.svg", format='svg')
    plt.close()
    return
```